The *n-XYTER* Reference Manual

— chip version 1.0 —

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Abstract

HUHNHUHN This paper describes in detail electrical specifications, operating conditions and port definitions of the readout chip *n-XYTER 1.0*. The ASIC development as a part of the EU-FP6 project DETNI within NMI3, is designed to be connected to three different, solid converter based neutron counting area detectors. They are to supplement future high intensity research applications at modern neutron sources. Each of these detectors is specified to house between 10^5 and $5 \cdot 10^5$ pixels in a single module with an overall neutron detection rate of up to 100MHz.

Because of the the statistical, non-triggerable nature of neutron data to be processed, the internal architecture of the chip is self triggered and data driven. It integrates 128 channels with low noise preamplifiers and shapers. Each channel has two different shapers with distinct time constants, one optimized for timing resolution, the other one optimized for energy (pulse height) resolution. A peak detector connected to the slower shaper allows for the application of a spectroscopic amplitude measurement.

An internal time stamp generator provides the temporal reference that may be employed to identify time coincidences of signals on different detector channels and thus correlate their spatial point of origin.

For testability and calibration purposes, a charge injector with adjustable pulse height was implemented. The bias settings and various other parameters can be controlled via a standard I^2C-interface.

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Document Edition History

This manual describes the *n-XYTER* chip versions 1.0, also known as DETNI

Version	Date	Author	Description
1.0	2006-06-28	ASB	document created

Chip Version History

Version	Submission Date	Changes relating to previous version
n-XYTER 1.0	June 2006	

1 Chip Architecture

The *n-XYTER 1.0* is a front-end detector readout ASIC that integrates 128 individual channels and a common sparcifying token-ring digital and analogue interface. It is particularly designed cope with high-speed statistical input signals of poissonian nature. To this end, the front-end part of the chip employs an asynchronous, data-driven architecture in which an analogue signal triggers the registry of a time stamp and the detection of the input signalt's pulse height. In this scheme, time stamp latching is triggered by a time-walk compensated discriminator. Both, the analogue pulse hight as well as the corresponding time stamp are stored into a four level deep fifo as a synchronizing interface.
The back-end part of the chip is clock synchronous. It realizes a token ring scheme in which busy channels are read out clock synchronously one after the other. The token ring together with the per channel FIFOs inherently accomplish de-randomization, sparsification as well as readout-bandwidth distribution and bandwidth focussing functions. The system is thus able to process poissonian distributed data at an average per chip data rate of 32 MHz with a maximum of 10% dead time. A simplified schematic is shown in figure 1.

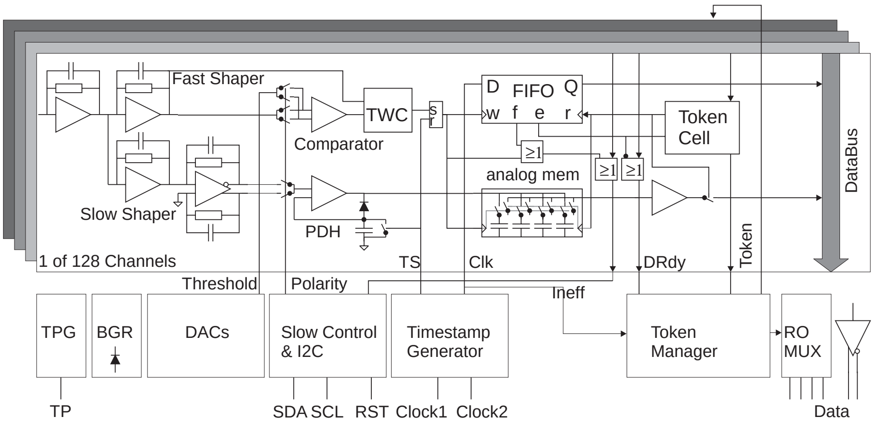


Figure 1: *n-XYTER* chip architecture. The upper part shows one of the 128 channels. In gray scale behind, more of the independent parallel input channels are suggested. The functional blocks at the lower part depict various controlling blocks of common infrastructure.

1.1 Front End

A charge sensitive preamplifier, constructed around a folded cascode circuit forms the input stage. For its superior noise performance, an NMOS input transistor has been chosen. Unlike conventional readout chips, the signal path is split into two branches after the preamplifier:

- A fast $\mathrm{CR}-\mathrm{RC}$ shaper, driving the timing-critical path. This branch serves to generate the time stamp and thus performs the time measurement. The time stamp may later be used to determine the time of incidence of the signal as well as to correlate signals on different channels like for example on the other coordinate in order to determine the eventt's locus in two dimensions.

- A slow $\mathrm{CR} - (\mathrm{RC})^2$ shaper driving the more noise-critical measurement of the deposited energy.

While the fast branch relies on a single-ended topology for the shaper, the slow branch is a two-stage design with a fully differential second stage. This allows the selection of the adequate signal polarity for the subsequent peak detector and hold circuit (PDH) for both polarities of the input signal. The PDH can only take positive input pulses.

Some frontend simulations show the transient response of all these stages when an input charge of $\pm\ 1\ fC, \pm\ 2\ fC, \pm\ 4\ fC, \pm\ 8\ fCor \pm\ 16\ fC$ is injected into the pre-amplifier. Figures 3 to 6 show the simulated transient response of the analogue front end at different stages in the circuit and for positive as well as negative input charges. The precise transient response does depend upon the values of the internal registers which define the analogue operating conditions. Settings for positive and negative input charge differ in order to maximize the dynamic range within the given clipping margins. Effectively the dc operating level of the fast shaper amplifier output is shifted between 0.56 V and 1.2 V. V_{cg} is set to 1.4 V and determines the pre-amp bias current, $V_{bfb} = 0.9\ V$ controls the pre-amp feedback circuitry and $V_{cm} = 1.1\ V$ is the slow shaper's common mode output level. A schematic of the front-end is shown in figure 2.

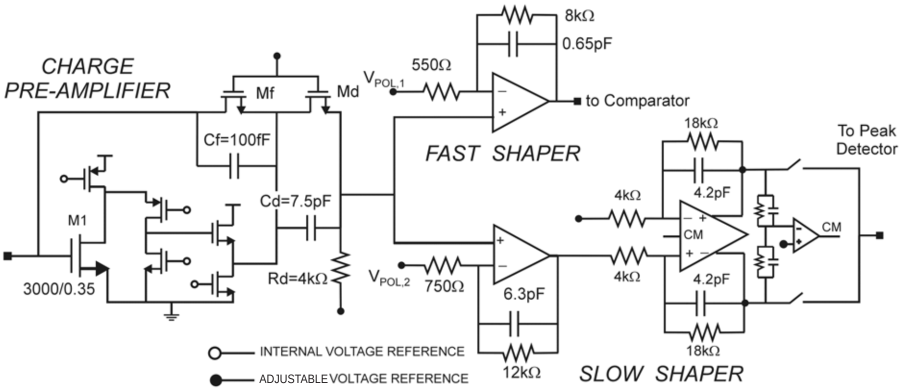
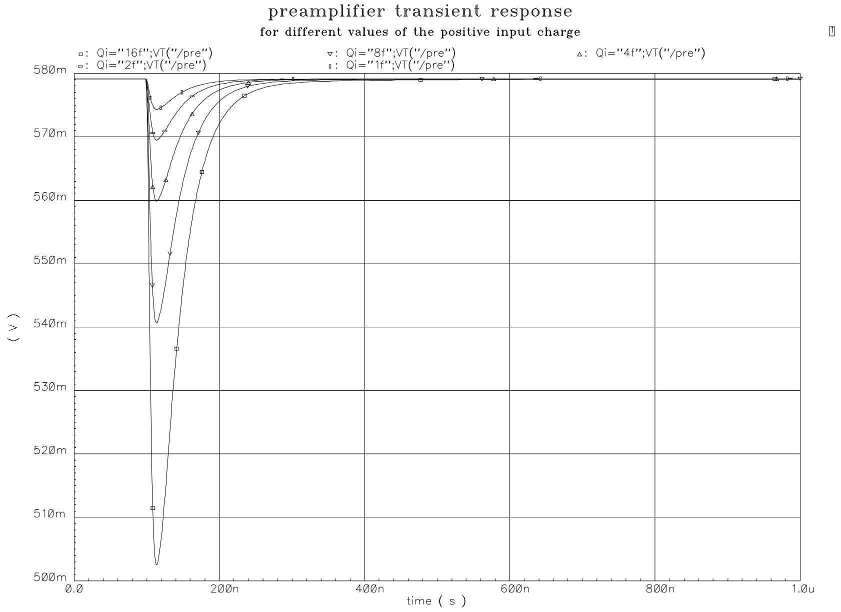


Figure 2: Schematic of the front-end, including FAST and SLOW shaper branches.

Table 1: Internal register contents for the simulations of transient responses. The register settings determine the values of working parameters for the internal nodes as well as a general configuration.

reg. number	register name	pos. charge	neg. input charge, all ch. on	neg. input charge, only testch.
0 -15	Mask reg		0	0
16	I_{cg}		160	160
17	I_{cgfoll}		255	255
18	V_{th}		-	-
19	V_{bfb}		6	0
20	V_{biasF}		74	95
21	V_{biasS}		77	125
22	V_{biasS2}		100	100
23	V_{cm}		137	137
24	cal		-	-
25	I_{COMP}		69	69
26	I_{DUR}		15	15
27	I_{INV}		54	54
28	I_{PDH}		92	92
29	I_{TWC}		69	69
32	config 0		0	1
33	config 1		12	11

Figure 3: Transient response of the pre-amp.



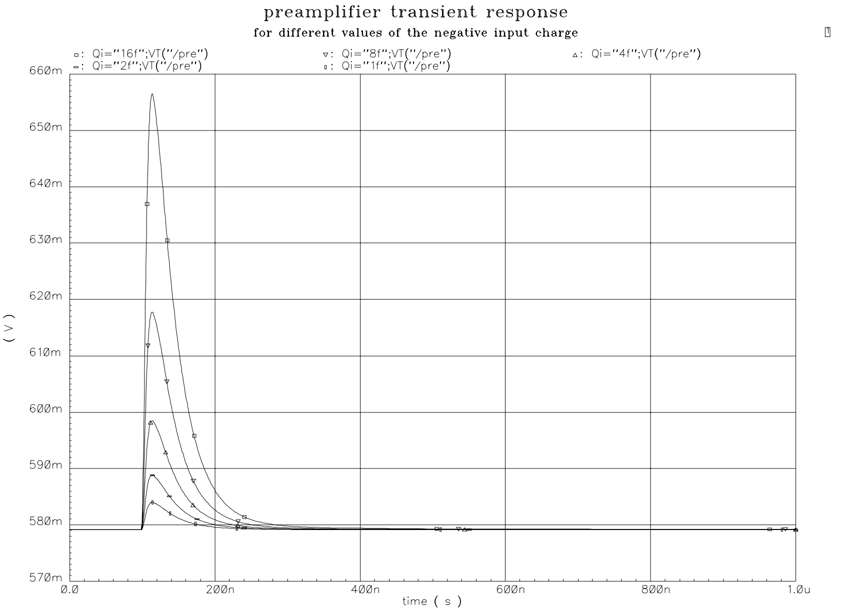


Figure 4: Transient response of pre-amp and fast shaper.

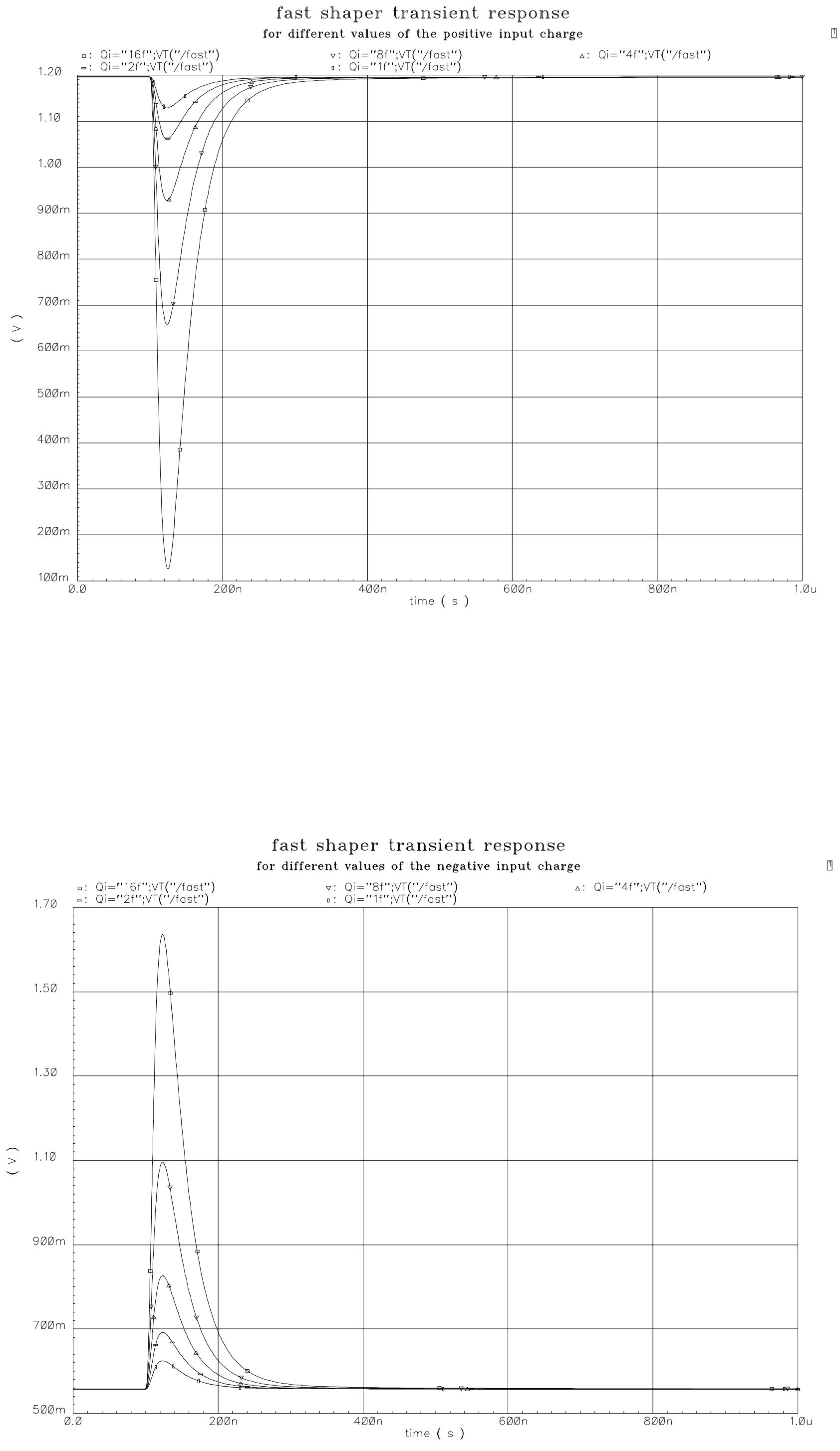
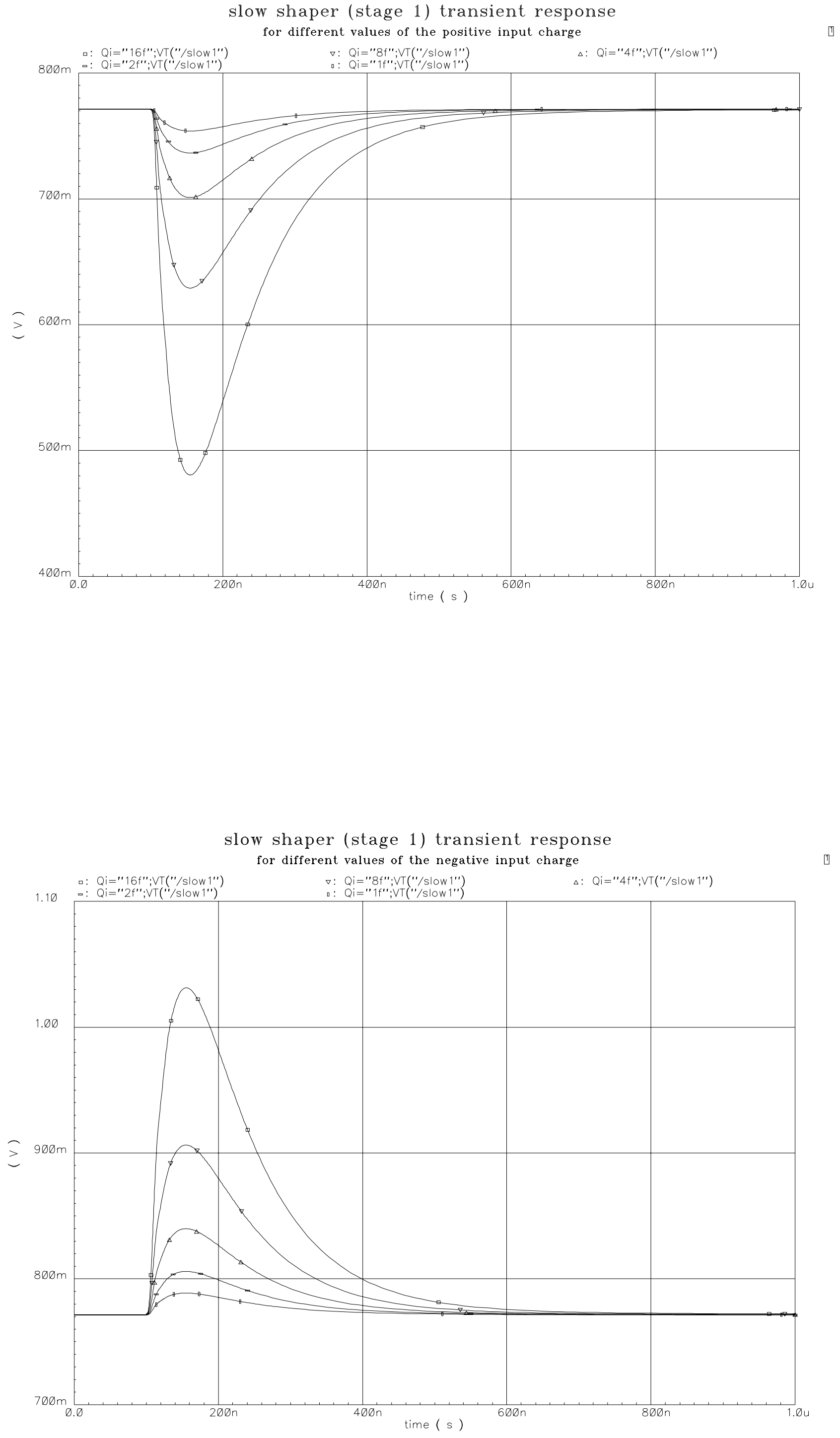


Figure 5: Transient response of pre-amp and slow shaper (1^{st} stage).



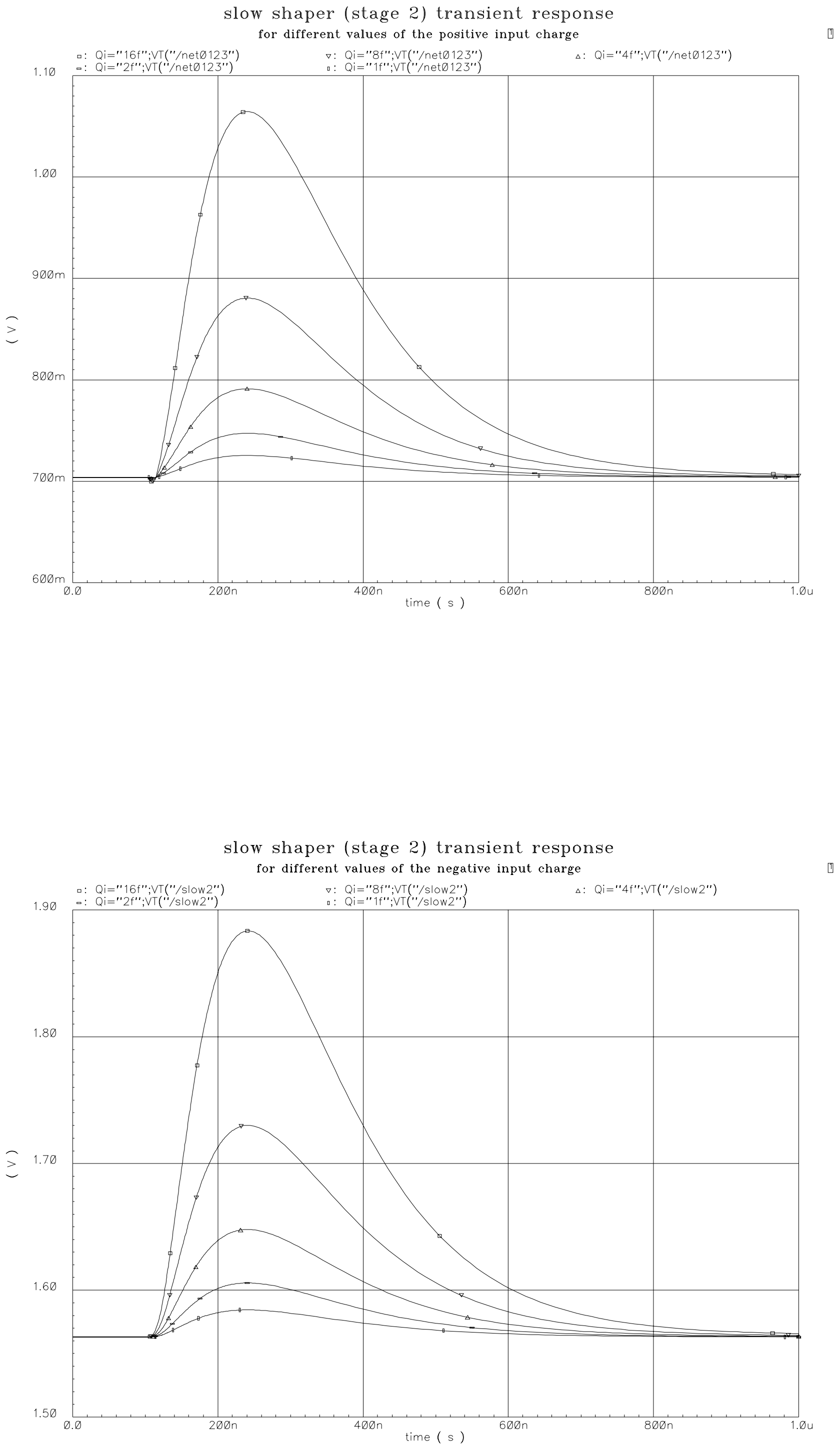


Figure 6: Transient response of pre-amp and slow shaper chain.

2 Electrical Specifications

2.1 DC Characteristics

Typical values for the power consumption of the *n-XYTER* chip are given in table 2. Nominal register settings can be found in Table 6. These register settings are intended to give a starting point for optimization. The nominal clock frequency is 250 MHz. It may be altered too, and in particular reduced if desired

Table 2: DC characteristics of *n-XYTER*

Supply	Min. [V]	Nom. [V]	Max. [V]	I [mA]	Description
vdda	3.0	3.3	3.6	513	Positive analogue supply (front-end)
vddmono	3.0	3.3	3.6	182	Positive analogue supply (monostable)
vddcomp	3.0	3.3	3.6	128	Positive analogue supply (comparator)
vddbuf	3.0	3.3	3.6	82	Positive analogue supply (output buffer)
vdd!	3.0	3.3	3.6	2	Digital power supply

These values are estimated from simulations, as well as determined from real consumption of the chip in different operating modes.

2.2 Power Dissipation

The data listed in the following section was determined with specific settings for operation chosen: All channels were active, the chip was set for negative input signals. The values are intended to give an impression on the power consumption experienced with the chip experimentally.

Current consumption all ch. on	753 mA
Current consumption all ch. off	359 mA (digital and readout infrastructure)
Total current consumption analogue frontend	406 mA
Current consumption per channel	3.15 mA
Power consumption per channel	10.4 mW
Expected power consumption	12 mW

Table 3: Power consumption of the different power nets as current sunk at 3.3V

	Vdd analog	Vdd Comp.	VDD Buffer	Vdd Digital	Vdd Mono-stable	Sum	Actual (total current consumption)
1 power net open	589mA	115mA	37mA	99mA	10mA	850mA	764mA
1 power net closed (power consumption of the closed net)	596mA	40mA	37mA	99mA	4mA	776mA	764mA

3 Operating *n-XYTER*

3.1 Front-end Pulse Shape

The front-end output signal is a semi-Gaussian pulse which can be characterized through three parameters:

- peaking time t_p $(0 - 100\%)$ or rise time t_r $(10 - 90\%)$,
- peaking voltage $\mathrm{V_p}$ and
- remainder R, which is the ratio between the signal voltage 25 ns after the peak (V_{25+}) and V_p.

The peaking time is sometimes hard to measure since the starting point of the pulse is not well defined, so the rise time t_r $(10-90\%)$ is usually quoted. Figure 7 explains the various parameters.

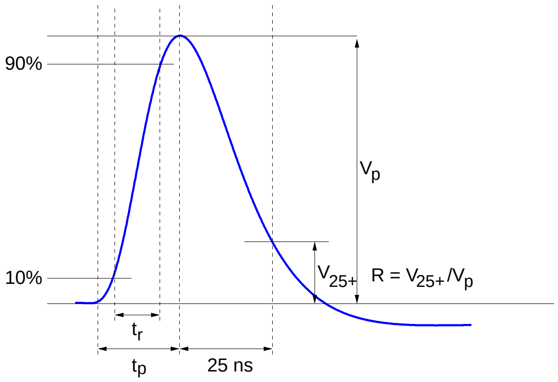


Figure 7: Semi-Gaussian pulse with the corresponding parameters characterizing shape.

The analogue pulse shapes of the *n-XYTER* readout chip may be observed on the test channel outputs (`fast`, pad no. 336, and `slow`, pad no. 326).

The pulse shape can be manipulated by means of 5 bias parameters. For practical operation, three of these are essential, as they control the output signal DC-levels of the pre-amplifier as well as the two shapers:

Vbfb sets the preamplifier bias voltage. Higher voltages decrease the rise time and the remainder and increase pulse undershoot.

VbiasF defines the shaper dc output voltage level. Increasing voltage shifts the DC-offset to lower values and results in slightly decreasing rise time, remainder and undershoot.

VbiasS sets the slow shaper dc output voltage. It does not affect the shape of the pulse, but the DC-offset.

4 Configuration and Control of the *n-XYTER* , Slow Control

n-XYTER contains 46 8-bit registers that may be accessed, programmed and read out via an I^{2}C slow control interface. These 46 registers are assigned the I^{2}C addresses 00 – 45. Table 4 coarsely lists and groups these registers in a register-map.

Table 4: I^{2}C Registers

I^{2}C Address	Register
0 – 15	Mask registers
16 – 29	Analogue bias and analogue front-end configuration registers
30 – 31	spare
32 – 33	General configuration register
34 – 35	Overflow counter, readonly, reset after readout
36 – 37	Missing token counter, readonly, reset after readout
38	Test pulse delay register
39	Test trigger delay register
40	spare
41	spare
42	Trim DAC shift register (bit 0..4), channel shut down on bit 5
43 – 45	Clock delay registers

4.1 I^{2}C Interface

The chip's slow control interface is a standard I^{2}C-slave device featuring a transfer rate of 100 kbit/s. The chip address, necessary to access a single device via the I^{2}C-bus, is 7 bits wide and assigned via the address pads `I2C_ID<6:0>` (c.f. section B.3). The *n-XYTER* chip may be given any address in the range $8-119$. The addresses `0000XXX` and `1111XXX` are reserved in the I^{2}C-standard for other purposes [3].

The internal registers may be accessed via a *pointer register*. It contains the address of the register to be written or read first. Only the 6 least significant bit (LSB) of the pointer byte are evaluated. The pointer is internally incremented by 1 after each transferred data frame (auto-increment). In this way registers with adjacent addresses may be accessed consecutively. The pointer register itself remains unchanged, i.e. a new transfer will start at the original pointer position. Figure 8 explains the transfer sequences in write and read mode. Data is always transferred with the most significant bit (MSB) first. In write mode, the chip address is transmitted after initializing the transfer, followed by the pointer byte and the data. After transmission of one data frame, the pointer addresses the subsequent register because of its auto-incrementing function. Transfer of the pointer byte is obligatory in write mode.
In read mode there are two versions:

- Preset pointer
  After initializing the transfer and sending the chip address, data is immediately read out. The pointer has been set in a previous transfer.
- Pointer set followed by immediate read-out
  After initializing the transfer and sending the chip address the pointer byte is transferred. The I^{2}C-bus is re-initialized, the chip address is sent and data is read out.

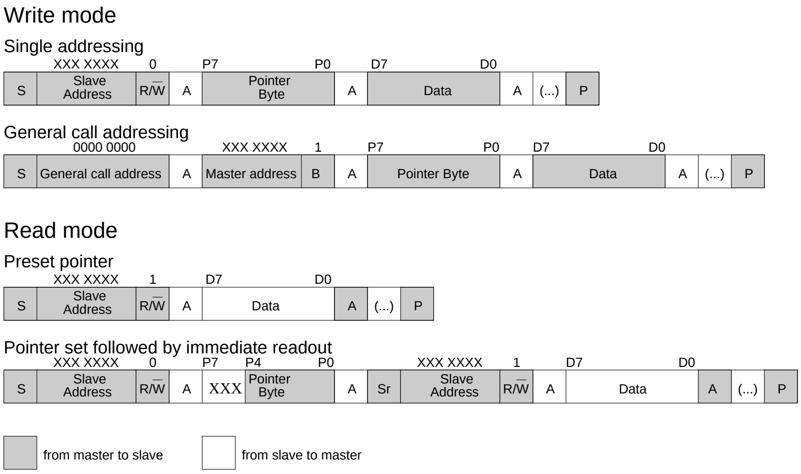


Figure 8: I^{2}C-bus write and read sequences for accessing slow control registers on the *n-XYTER* .

Caveat: In this version of the n-XYTER, the auto-increment function of the I^{2}C is not adequately adapted: Upon writing, auto-increment is turned off for or passing registers 28 and 29. Additionally, auto increment is operative only on a maximum of 64 addresses, which however is not relevant for the chip discussed in here. Upon reading, auto-increment does work for all register addresses up to 46. These issues may be entirely avoided if registers are individually addressed, thus avoiding auto-increment features.
Commercially available I^{2}C-devices usually operate at 3.3 V or 5 V. Because the *n-XYTER* is a 3.3 V circuit it is necessary to use an adapter to operate with 5 V. A simple FET level-shifter with local bus pull-ups to the respective operating voltage level on either side may be employed.
The following subsections list the registers with their physical range, resolution, nominal setting and power up default settings.

4.1.1 Mask Registers

The Mask Register is a 128 bit length register which is accessible in parts of 8 bits width via the I^{2}C registers 0 to 15 as shown in Table 5. In particular, the channels from 0 to 7 are masked by bits from 0 to 7 of register 0 and channels from 120 to 127 are masked by bits from 0 to 7 of register 15. When a channel is masked the corresponding bit is set to 1, the output of the front-end does not propagate to the back-end and no event is registered at the output in any mode of operation.

Table 5: I^{2}C Mask Registers

Reg. No	Description
0	Mask channels 7-0
1	Mask channels 15-8
2	Mask channels 23-16
3	Mask channels 31-24
4	Mask channels 39-32
5	Mask channels 47-40
6	Mask channels 55-48
7	Mask channels 63-56
8	Mask channels 71-64
9	Mask channels 79-72
10	Mask channels 87-80
11	Mask channels 95-88
12	Mask channels 103-96
13	Mask channels 111-104
14	Mask channels 119-112
15	Mask channels 127-120

4.1.2 Bias Registers

Registers 16−29 are bias registers that serve to tune and control the analog front-end stages. Apart from general best settings that need no repeated optimization for most parameters, the parameters **VbiasF** and **VbiasS** as well as **Vbfb** need to be set upon a change of the polarity of the input pulses that are to be detected:

Icg (16) (named **Vcg** in the schematic): This is a pre-amplifier parameter that ...

Icgfoll (17) (named **Vcgfoll** in the schematic) sets the bias voltage for the shaper (together with VbiasF) and both stages of the slow shaper (together with VbiasS and VbiasS2 in this case). For more information about these voltages check the paragraphs on VbiasF, VbiasS and VbiasS2.

Vth (18) sets the global threshold voltage for the comparators, i.e. it defines the pulse strength that is necessary to trigger the comparator. Two voltages are created for positive and negative input charge: vt1 and vt2. These discriminator input voltages are selected depending upon the front-end polarity setting in configuration register number 33, bit 2.

Vbfb (19) Sets the discharge time for the preamplifier by controlling the resistance of the transistors Mfb and Mpz. Vbfb is also the upper limit for the output voltage. A large negative charge as input produces a large positive output signal that might be cut through if Vbfb is set too low. Nevertheless, increasing Vbfb will decrease the discharge resistance and result in greater noise and undershoot. It also decreases the rise and discharge time.

VbiasF (20) sets the bias voltage for the fast shaper (together with Icg). It serves to set VcommonF, and thus modifies the dc offset of the shaper output. The potential of VcommonF may be observed at the respective test pin. VcommonF is connected over the two packages of resistors RcFa (R0, R5, R2, R3) and RcFb (R21, R22, R23, R24) and a capacitance (C16) to the output of the fast shaper. A change in VcommonF is reflected in the output with the following multiplier: $1 + (RcFb/Rcfa) = 17$. So the fast shaper is very sensitive to pickup in VcommonF. VbiasF should be used to adjust the bias voltage of the output. For a negative input charge the resulting signal is positive and its bias should be around 0.5 V so that there is enough space for the upward swing. For a positive input charge the signal is negative and its bias should be around 1.2 V so there is enough space for a downward swing.

VbiasS (21) sets the bias voltage for the first stage of the slow shaper (together with IcgFoll). It also sets VcommonS, which can be measured at the respective test pin. The working principle is exactly as with VbiasF, even the multiplier is identical. Only the bias value of the output (of the first stage of the slow shaper) is different.

VbiasS2 (22) together with IcgFoll sets the bias voltage for the second stage of the slow shaper. It also sets VcommonS, which can be measured at the respective test pin and should be identical with the input bias voltage (which is the output of the first stage of the slow shaper). Since this cannot be measured the following can be used: If they are identical, the second stages slow shapers output bias voltage is identical for positive and negative charges. A difference can also be caused by a wrong setting for Vcm/Vbase.

Vcm/Vbase (23) : The output of the slow shaper is differential. Vcm/Vbase adjusts the target voltage of the common mode feedback that stabilizes the output. It should be the same as the bias voltage of the output of the slow shaper second stage.

cal (24) : If the chip is in "test pulse mode" (c.f. configuration reg. 32, bit 0), an internal pulse can be created and fed to the analog channels, thus enabling testing of the chip without external input. Register 'cal' sets the strength of this pulse.

iCOMP (25) sets the current for the main stage of the comparator.

iDUR (26) adjusts the dead-time of the analog channels, i.e. the minimal time difference between two events so that both will be distinguished as two signals on one channel. Upon occurance of a new trigger piling up on a previously registered signal within the pre-defined dead time, only one signal will be registered, where the analogue pulse height must be considered contaminated. This data element is then marked as "pile-up".
This timing logic is realized by means of a mono-stable, which is activated through the trigger signal. iDur sets the discharge current and thus the time-window width of the mono-stable, which in turns arms a watchdog-logic to check for a coincidence during this time span. The larger the programmable current

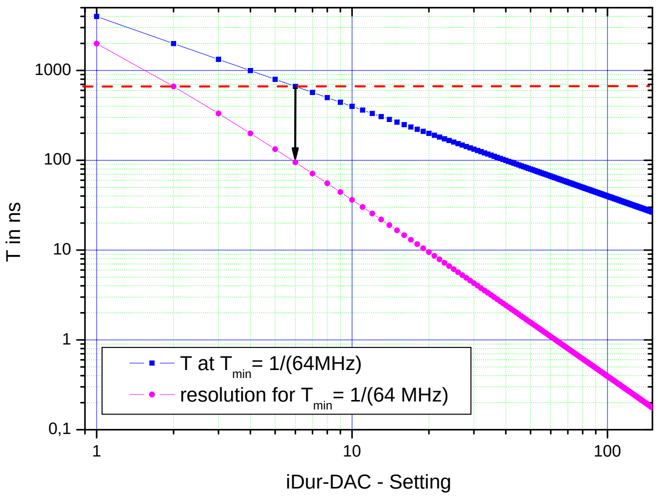


Figure 9: Variable dead time and its resolution as a function of the iDur parameter

iDur, the shorter the window.
The width of the time window is given by:

$$T_{dead}[ns] = \frac{4790}{DAC} + 250 + (31.25 \text{ synchronization jitter})$$

Since the dead-time is an adjustable parameter, it may be employed to study signal saturation and detector performance. Note though, that the dead-time introduced here must be considered non-re-triggerable dead-time.

iINV (27) sets the current in the output stage of the comparator.

iPDH/iOTA (28) sets the current in the peak detect and hold circuit.

iTWC (29) sets the current in the time walk compensation circuit.

4.1.3 Configuration Registers 32 and 33

The Configuration Register are two successive 8 bit registers accessible trough the I^2C registers 32 and 33. Tables 7 and 8 describe how they control the internal configuration of the chip.

4.1.4 Overflow Counter, Registers 34 - 35

The diagnostic overflow counter contains the current number of the events lost due to FIFO overflows since the last reset of the counter. The Overflow counter

Table 6: Bias and configuration registers of *n-XYTER* .

Reg. no.	Reg. Name	Range	Resol. of LSB	Nominal Setting		Description
				Value	Reg. content	
16	*Icg*	128 - 270 µA	0.573 µA	187 µA	`114`	bias current
17	*Icgfoll*	0 - 214 µA	0.835 µA	124 µA	`151`	source follower bias current
18	*Vth*	(vdd) - (vdd-862 mV)	3.42 mV	— µA	`--`	comparator threshold voltage
19	*Vbfb*	0.928 - 1.851 V	3.66 mV	1.2V	`80`	preamplifier voltage
20	*VbiasF*	0.928 - 1.85 V	3.73 mV	1.27V	`103`	fast shaper voltage
21	*VbiasS*	1.031 - 1.640 V	2.55 mV	1.27V	`113`	slow shaper voltage
22	*VbiasS2*	1.031 - 1.640 V	2.51 mV	1.129V	`44`	slow shaper voltage
23	*Vcm, Vbase*	0.825 - 1.581 mV	2.97 mV	1.1V	`103`	common mode voltage
24	*cal*	1.381 - 3.00 V	-6.35 mV	2.0V	`100`	voltage calibration
25	*iCOMP*	0 - 214.2 µA	0.843 µA	62.1 µA	`62`	current bias for comparator
26	*iDUR*	0 - 65.4 µA	0.657 µA	0.657 µA	`15`	current bias
27	*iINV*	0 - 260.1 µA	1.02 µA	37 µA	`37`	current bias
28	*iPDH, iOTA*	50.5 - 139.2 µA	0.349 µA	80 µA	`92`	current peak detector
29	*iTWC*	0 - 214.2 µA	0.843 µA	60 µA	`75`	current time walk compensation
30	*reserved*	-				
31	*reserved*	-				

is a 16 bit register accessible thought I^{2}C registers 34 and 35. These are read only registers and are reset after read. The reset is synchronous with reading, once 8 bits are read, they are set to 0 (all bits are 0). After 2 readings (consecutively on register 34), all bits are set to 0.

4.1.5 Missing Token Counter, Registers 36 - 37

This diagnostic counter contains the current number of tokens lost since the last reset. The Missing Token Counter is a 16 bit register accessible trough the I^{2}C registers 36 and 37. These are read only registers and are reset after read. The reset is synchronous with reading. Once 8 bits are read, they are set to 0. After 2 consecutive readings on register 34, all the bits are set to 0.

4.1.6 Trim DAC Shift Register 42: Local Threshold and Individual Channel Shut-Down

The Trim-DAC Register may be employed to equalize the offset and gain mismatch of effective local thresholds. For every channel, a 5 bit corrective adjustment value may be tuned to add to the global threshold. Additionally, register 42 provides a switch to individually shut-down any one or more front-end channel.
The implementation consists of a 129 stage shift register, one for each channel. Each channel has its corresponding 1 byte local register with bit 0 to 4 controlling local threshold correction and bit 5 being the channel shut-down bit (bit 5

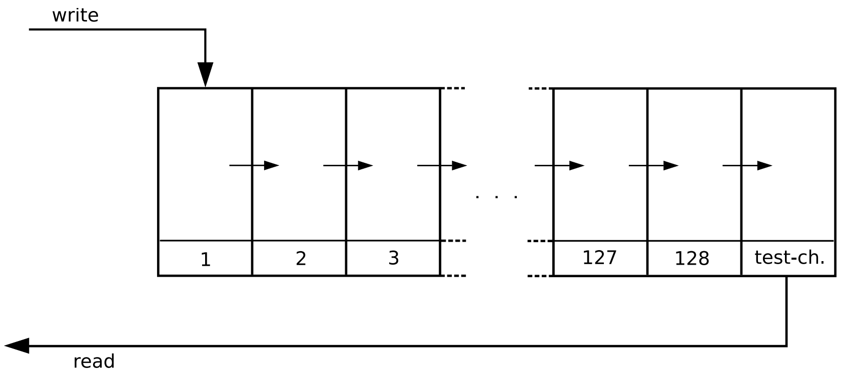


Figure 10: Shift register principle

= 1 shuts off the channel).
A write command on register 42 addresses the first one of the chain, the location of channel 127. A read command on register 42 reads from the very last item, the position of the test channel, which is located just next to input channel 0. To set the values of the DACs, a sequence of 129 writing commands to register 42 needs to be send. Each writing pushes another 8 bits into the shift register, where previous values are pushed through to sucessive channel numbers. In order to read the entire shift register, 129 alternating read- and write-actions must be performed. The first one read will correspond to the test channel, no. 129, the last one to channel no. 1 respectively.
If e.g. location number 50 is to be read out while maintaining the content of the shift registers, the entire shift register needs to be read out by alternating read and write commands to register 42, that write back the very value just read out. The principle of the shift register is shown in Figure 10.

Upon bit 5 set to 1 in the Trim-DAC register of any channel, power in the respective channel is cut off from the pre-amplifier, the fast shaper, the first stage of the slow shaper as well as the second stage of the slow shaper. Figure 20 and the successive schematics of the hierarchy in Appendix **??** show the electrical connections of the `shtdwnneg` signal which is controlled through bit 5 of the shift register entries.

4.1.7 Delay Registers

Signal delays may be introduced and controlled in various locations of the circuit. Such delays are programmed via I^2C delay registers. Registers 43, 44 and 45 are used for the clocking scheme. Registers 38 and 39 are used to shift test signals in dedicated test modes with respect to the clock. These delay registers are inverter based delays as depicted in figure 11 and have a typical delay of about 100 ps per bit. Note that the effective delay is asymmetric between a rising and a falling edge. The internal structure of the delay buffers is presented in figure 11. The effective delay of the buffer may be programmed by attaching capacitive loads to the outputs of four serially connected inverters. Note that pairs of capacitors are connected serially to optimize minimum delay of the buffer. Thus setting e.g. bit 1 while bit 0 is not asserted does not alter the delay!

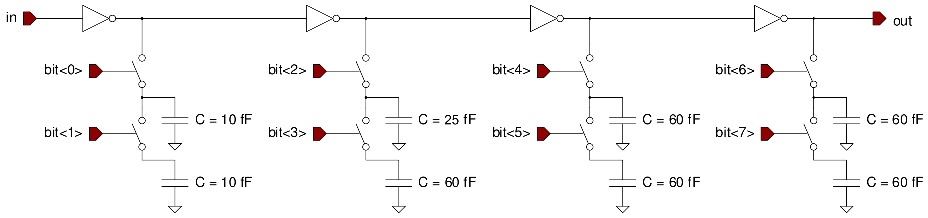


Figure 11: Simplified schematic of the delay buffer

The expected delay can be calculated with the following equations:

$$Falling\ Output = \frac{0.01\ ns + 2.00\ ns}{pF} \cdot C[pF]$$

$$Rising\ Output = \frac{0.21\ ns + 1.71\ ns}{pF} \cdot C[pF]$$

$$Average = \frac{0.11\ ns + 1.86\ ns}{pF} \cdot C[pF]$$

Falling Output is the logic transition from high to low and C is the load capacitance at the output of the inverter.
Rising Output is the logic transition from low to high and C is the load capacitance at the output of the inverter.
Average is the average value expected for a transition (from low to high or high to low) and C is the load capacitance at the output of the inverter.

The entire delay module consists of 4 inverters

$$td = \frac{0.44\ ns + 1.86\ ns}{pF} \cdot C_{tot}[pF]$$

where td is the total delay and C_{tot} the sum of all the load capacitance at the output of the inverters.

The plot in Figure *XX, (from test measurements)* shows the relationship between delay settings programmed into the registers and the resulting time delay between the clock phases. This measurement can be used to calibrate the delay and archieve proper time settings.

Test Pulse Delay Register 38 The test pulse delay register controls the delay of test pulse injection with respect to the clock, if clock synchronization is selected for the test pulse mode in configuration register 32, bit 1.

Test Trigger Delay Register 39 The test trigger delay register controls the delay between test triggering of the front-end's output and data registry and the clock if clock synchronous mode is selected in configuration register 32 bit 4. (C.f. figure 12.)

Clock Delay Register 43 The clock fed into the chip on the input clkA is split into two clock branches. This register controls a shift in time of the second clock branch with respect to clkA. It needs to be tuned to cause a phase shift of 90°between the two branches (See the diagram in figure 16). The delayed signal feeds into a D-flip-flop and is employed as gray coded time-stamp bit number 1.

Clock Delay Register 44 and 45 The output clock of Delay Register 44 is also fed successively into clock delay registers 44 and 45. Here the delays are chosen so that a real, homogeneous gray code is realized.

4.2 Signal Polarity Configuration

The *n-XYTER m*ay be configured to alternatively detect signals of positive or negative polarity.

Since the peak detector to which the energy signal is fed after the slow shaper may only analyze pulses of one polarity, the preceding second stage of the slow shaper is realized as an entirely differential circuit. Likewise, the discriminator that is fed from the fast shaper circuit, is realized entirely differential, so that depending upon the polarity of the connecting branch, either positive or negative signals may be discriminated or peak analyzed. The choice of the input channels of these differential internal circuits is controlled through bit 2 of Configuration Register 33. It controls the switches depicted in figure 1.

Front-end polarity select (bit 2 of Configuration Register 33)

- When **0**: Switch configuration for **negative** input charge.
- When **1**: Switch configuration for **positive** input charge.

Additionally, the front-end should be adapted for maximum dynamic range: Here configuration merely comes down to an adjustment of DC-operating levels that allow to exploit the entire analogue operating window for unipolar signals. To this end, the adjustable nodes in 2 may be set by means of I^{2}C registers. In particular the parameters `VbiasF`, `VbiasS` and `VbiasS2` as well as `Vcgfoll` are employed to set VcommonF, VcommonS and VcommonS2, the nodes depicted as adjustable in figure 2. VbiasS2 does however have little influence on the output dc level as compared to VbiasS. This is due to the fact that it is primarily the first stage that introduces gain in this shaper. Finally, `Vbfb` is adjusted as to optimize the pre-amplifier feedback time constant while keeping Johnson noise from the feedback resistance minimal. For positive and negative signals, the optimum shows slightly different values as in the Paul O'Connor dynamic pole zero circuit employed, the feedback resistance is modified by the signal level itself.

4.3 Test Channel

In addition to the 128 channels, the *n-XYTER* chip integrates a *test channel* that allows direct access to it's front-end's shaper outputs `fast`, pad no. 336, and `slow`, pad no. 326, as well as the comparator output `comp`, pad number 312. An input charge can be injected either via the test channels input port `Test_In` (pad no. 3) or via the internal test pulse generator in test pulse mode and addressing calibration group 11 (cf. 4.6). Additional connections `Vbfb` on pin 142 and 353, `icomp` on pin 179 and 316, `iINV` on pin 314 and `Uref` on pin 304 are also accessible to monitor or force an appropriate bias to the test channel. Please not that the dynamic output signals of the test channel shapers, and in particular the fast shaper, are not buffered. They need to be sampled with an oscilloscope probe of less than 1 pF input capacitance. Even connecting pcb-traces need to be designed for absolute minimum capacitance.

4.4 Channel Shutdown

The analog channel has a shutdown function which cuts off the power supply for the front-end, the fast shapers, the first stage of the slow shaper and the second stage of the slow shaper. It is not possible to switch off the individual components of a channel but the entire front-end at once. Figure 20 in appendix A shows the electrical connections of the `shtdwnneg` signal.

The channel is switched off individually, regardless of the on/off status of the adjacent channels. The shutdown is activated by writing a logic 1 in the trimdac register 42, bit number 5. The first entry of this shift register after writing to it 129 times controls the test channel. Thus the state of the test channel shift register entry is the first that is read out. The ordinary 128 channels are addressed and read out by successively writing into the shift register, entry 2 corresponds to channel 0 and entry 129 corresponds to channel number 127.

4.5 Reset Modes

Three different types of resets exist on the *n-XYTER* .

- *Time Stamp generator reset* pins 235/236 `Reset_PN` is an LVDS signal that asynchronously resets the time stamp generator. The counter of the timestamp is initialised to value 0 which means all bits are zero. The pulse width (a transition from low to high and then back to low) must be longer than 350 ps. This reset signal also serves to reset the down counter which is used to generate the lower frequency signals 128 MHz and 32 MHz. **For adequate operation of these data transmission clocks and in particular their relative phases and the phases with respect to the time stamp, a time stamp generator reset must be applied prior to operation.**

- *I^2C reset* is controlled by the `I2C_Reset` on pin 215. When active (it is active low), this signal resets the internal digital I^2C logic and the state machines, but not the values loaded in the I^2C registers. The contents of the registers 0 to 45 are preserved and their values do not change after activating this reset. It is recommended to apply the signal, being internally asynchronous, longer than one clock period.

- *I^2C registers reset* is controlled by the `RegReset` on pin 216. When active (it is active low) this signal resets all the registers of the I^2C. In this situation all registers are set to their default values. Hard wired default values are either 0 or 128.

4.6 Test Modes

The *n-XYTER* may be set to four different states of operation that are selected by means of bit 0 (test pulse enable) and bit 3 (test trigger mode) in the control register number 32.:

- With both bits inactive, 0, ordinary operation is selected. The discriminator signals of all unmasked channels are fed forward and processed.

- "Test pulse enable" enables the injection of test pulses into one of four groups of 32 channels (selectable through control register no. 33 bit 0 and 1). In this *test mode #0*) or *"test pulse mode"*, an external digital, single ended signal on the input "TestPulse" (pad 217) triggers the injection of test pulses if the control bit "test pulse enable" is selected. The generated signal is further processed just like an ordinary detector signal (see figure **??**). In this case, the mask register serves as a select register to close the switches at the inputs of selected channels (mask bit set to 1) so that the test pulse is coupled through a 100fF coupling capacitance into the respective channel input (see figure 13. It may be employed to mimic a detector signal where the precise time of injection is under control and directly correlated to the time of application of the external TestPulse signal. This test mode is further discribed in chapter 4.6

- If on the other side *test trigger mode* (or *test mode #1*) is chosen through control bit 3 reg. 32 set to 1, analogue front-end discriminator signals are inhibited from passing on to the digital readout. Here, the internal signal "test trigger" in figure **??**, likewise triggered by the external signal TestPulse, emulates a trigger signal on all unmasked channels. On the rising edge, the digital trigger and the time stamp registry is forced. Further, the peak detector is activated on these channels to sample the analogue energy signal. On the falling edge of the external TestPulse, the momentary states of the discriminators are latched into a register that is mirrored onto the mask register read addresses. The precise time of the sample may thus be controlled through the length of the TestPulse digital signal.
  This test-mode emulates simultaneous firing of many (up to all 128) discriminators. This feature and the test mode as a whole were added as a back-up diagnostic tool that allows to investigate the front-end even if the back-end was faulty, or likewise to investigate the back-end if the front-end was inoperative. With test pulses enabled (bit 0 of control register 32 set to 1), test pulses may be injected into the front-end also in test trigger mode.

- Additionally, with test pulses disabled, this test trigger mode may be employed to realize an analogue base-level measurement for every channel,

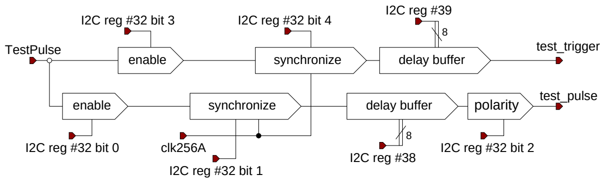


Figure 12: Generation of test signals.

as upon a trigger signal on TestPulse, all non-masked channels are forced into taking an analogue sample of the signal with the respective peak detector, which may then be read out.

Note: When test_pulse is disabled, all the switches at the inputs of the front-end channels are opened (compare with figure 13). The test pulse generator is not only inactive but rather entirely disconnected.

The generation of the test signals is depicted in figure 12. Both signals originate from the external `TestPulse` pad (pad 217) and are enabled by appropriate configuration bits, as shown in the figure. The signals can be synchronized on the rising edge of the `clk256A`, and delayed by setting the I2C registers 38 and 39. The `test_pulse` signal polarity can also be controlled by a configuration bit.

4.7 Internal Test Pulses

An internally generated test pulse may be coupled into every channel of the ASIC when test pulse enable is selected (configuration register 32, bit 0 set to 1). The amount of charge injected is controlled through register *cal* (reg. 24). One of four test pulse generators is activated and sends test pulses to the channels belonging to one of four groups of 32 channels, selectable through configuration register 33, bits 0 and 1 (see table 8). For the test pulse to be injected into any channel, the channel additionally needs to be connected to its respective coupling capacitor. This is done by means of the mask register. A mask bit 1 disconnects the channel (see figure 13).

The last requisit for a test pulse to be injected is a positive edge on the single ended digital input “TestPulse” (input pad 217). The test pulse may be issued synchronized to the clock (configuration register 32 bit 1 set to one) or entirely asynchronous. Further, when synchronous, it may be issued delayed with respect to the clock (delay register 38 bits 0–7). Its polarity is determined through configuration register 32 bit 2 (0 corresponds to positive charge, 1 to negative charge). The control scheme of the test pulse generation is depicted in figure 12.

Note: The test channel cannot be masked and belongs to the group of channels selected by configuration register 33 bits 0–1 being set to 11.

In response to a full swing square wave at the strobe input TestPulse, the

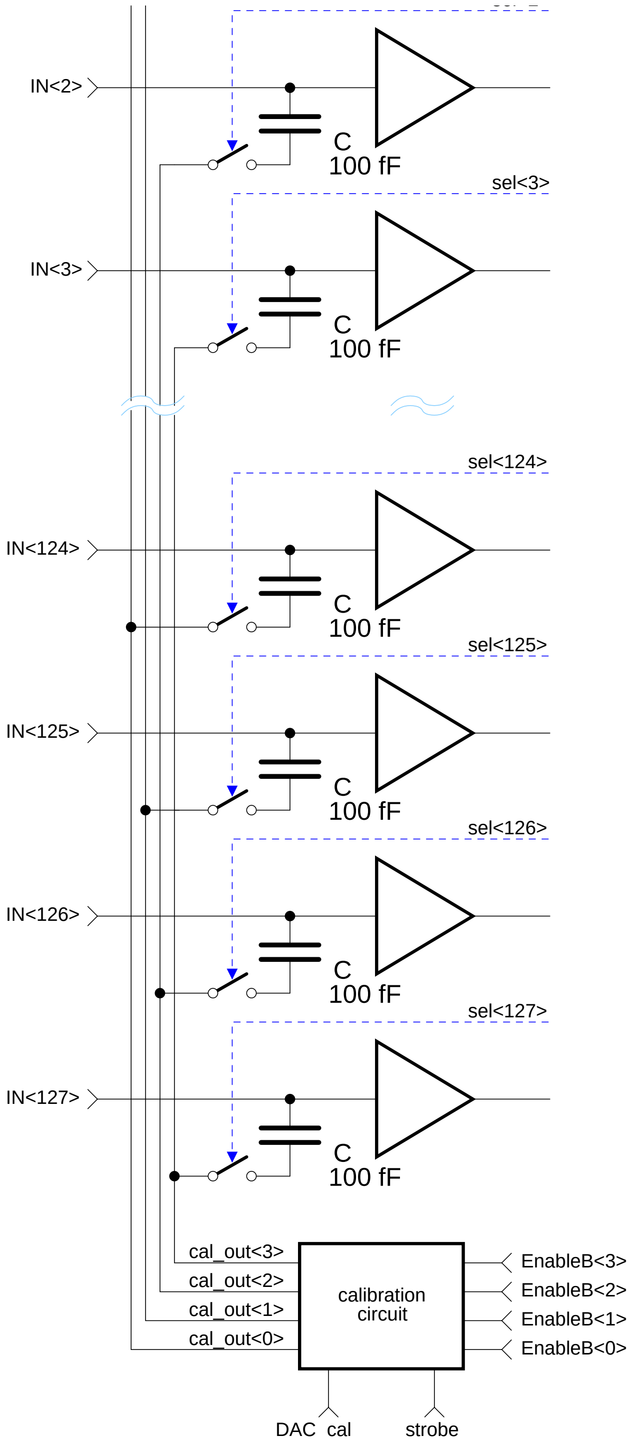


Figure 13: Block diagram of the connection between calibration circuit and channel inputs. The signals sel(127:0) are controlled through the mask registers (I^2C reg. 0 - 15), EnableB(3:0) correspond to configuration register 33 (bits 0 and 1) and the digital signal strobe corresponds to the externally applied signal TestPulse (pad 217)

calibration circuit generates voltage steps across the capacitor coupling into the channel input. The test capacitor of C=100 fF is stimulated with a voltage step that injects the charge $Q = C \cdot \Delta V$. The step height may be programmed through I^{2}C register 24 **cal** from 0 to 1.137 V.

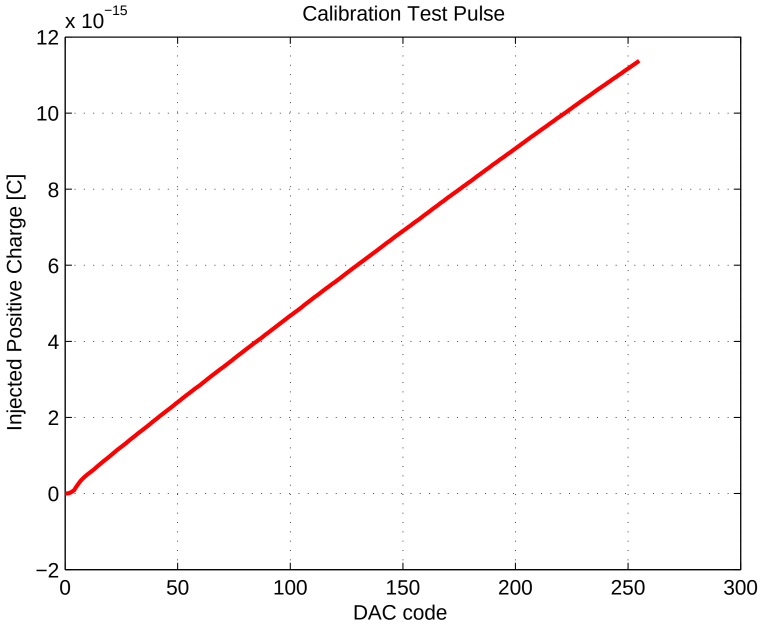


Figure 14: Injected positive charge during the calibration procedure.

The corresponding injected charge at the input of the preamplifier is variable in 256 steps from 0 fC to 11.37 fC. The amount of charge injected as a function of cal-register setting as simulated is displayed in figure 14 for positive charge and figure 15 negative charge.
The least mean square approximation with a linear function of the calibration curve yields a DAC gain of 44.63 aC/LSB for the positive charge and -44.55 aC/LSB for the negative charge with 0 C offset for positive charge and 0 C offset for the negative charge.

Least mean square linear function fitting curve:

$$\texttt{positive test charge}[C] = \frac{44.52\ aC}{LSB} \cdot Reg24Value[LSB] + 162.7\ aC$$

$$\texttt{negative test charge}[C] = \frac{-44.41\ aC}{LSB} \cdot Reg24Value[LSB] - 182.0\ aC$$

,

where Reg24Value[LSB] is the value written into the cal register (I^{2}C register 24).

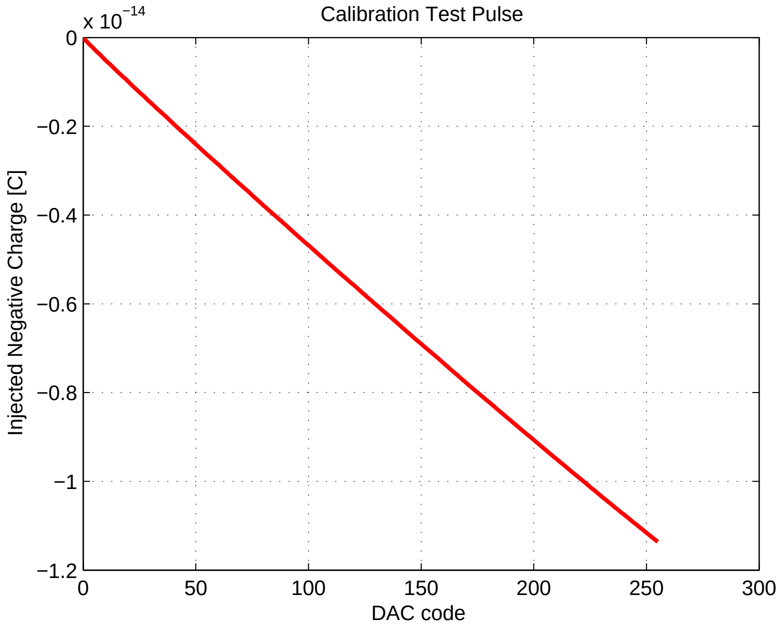


Figure 15: Injected negative charge during the calibration procedure.

4.8 Comparator Operation and Time Walk Compensation

The comparator circuit consists of an integrator, a threshold generator and a discriminator. The integrator tracks the DC-offset of the shaped pulse with a variable time constant

To correlate the signals on the x- and y-plane of a detector by means of a time stamp, a discriminator has to detect these signals without any dependency on the signal amplitude. A single pulse discriminator is followed by a voltage controlled delay circuit, which is used to compensate the time walk. With this circuit a reduction of the comparator's time dependency to less than 2 ns has been achieved.

The output of the *time walk* compensation circuit is not only used to latch a 14 bit time-stamp, but also to arm the peak detector and hold circuit connected to the slow channel.

The DC-offsets vary from channel to channel. It is added to the threshold voltage. The threshold level is adjustable with a resolution of 5 bits per channel.

4.9 Clock Signals

The *n-XYTER* is fed with a clock signal of nominally 256 MHz. It is used to run the internal digital circuitry as well as to generate data transmission clocks 128 MHz and 32 MHz. Finally, clock *clk256* is used to generate a time-stamp of 1 *ns* resolution and to synchronize test pulses.

The chip has two clock inputs (LVDS):

- *clk256A* is the main clock. It is employed for time stamp generation, sychronization of internally generated test signals (test_pulse and test_trigger) and for readout clock generation.

- *clk256B* is the secondary clock. It is used for an alternative readout clock generation as well as an alternative time-stamp LSB generation.
  The configuration is set through the configuration registers 32 and 33. Functions:
  - **time stamp LSB generation** It may be selected, whether *clk256A* or *clk256B* should be used to derive the LSB of the time stamp. This is done by setting the *TSB LSB clock select* bit (Configuration register 32, bit 7) to 0 (derive LSB from *clk256A* on chip) or logic 1 (derive LSB from *clk256B*). The latter option was provided as an alternative, should one encounter any difficulties in shifting *clk256A* on chip. A - 90°phase shifted clock signal *clk256B* needs to be applied externally in this case (c.f. 16).
  - **synchronization of the test signals** (test_pulse, test_trigger)
  - **readout clock generation** (see next section for details)

4.9.1 Time Stamp Generation

Upon registry of a signal, a time-stamp is issued and registered to be stored in the respective channel FIFO together with the analogue signal peak height. This time-stamp is generated by means of a gray-encoded counter, the state of which is latched upon a trigger as the momentary time-stamp.
The homogeneous 14-bit time-stamp is built up from a 12-bit gray-encoded counter (bits 13:2), a toggle flip-flop (bit 1) and the buffered input clock (bit 0). With the adequate phase relation between bits 0, 1 and 2, a homogeneous 14-bit time-stamp counter is set-up.
The mechanism of time-stamp generation provides some alternatives that may be programmed. The simplified block schematic depicting the time stamp generation circuit is presented in figure 16.

The right timing between bits 1 and 2 is achieved by setting I^{2}C register 43 to appropriate values. A phase shift by -90°should be achieved on bit 1. The timing between bit 0 and 1 may be controlled through registers 44 and 45. Here, also, the signal needs to be shifted by -90°with respect to itself.

The clocks for chip operation can be generated in two ways, described in table 11: The *clk256A* LVDS input may be used in combination with *clk256B* according to the value of *TS LSB clock select* (bit 7 of Configuration Register 32). When *TS LSB clock select* (bit 7 of the Configuration Register 32) is low (0) the LSB of the time stamp is derived from *clk256A*, if it is high (1) the LSB of the time stamp is derived from *clk256B*.

If the *n-XYTER* is to be operated with just one input clock,*clk256A*, bit 7 of Configuration Register 32 should be set to 0 so that the LSB of the time-stamp

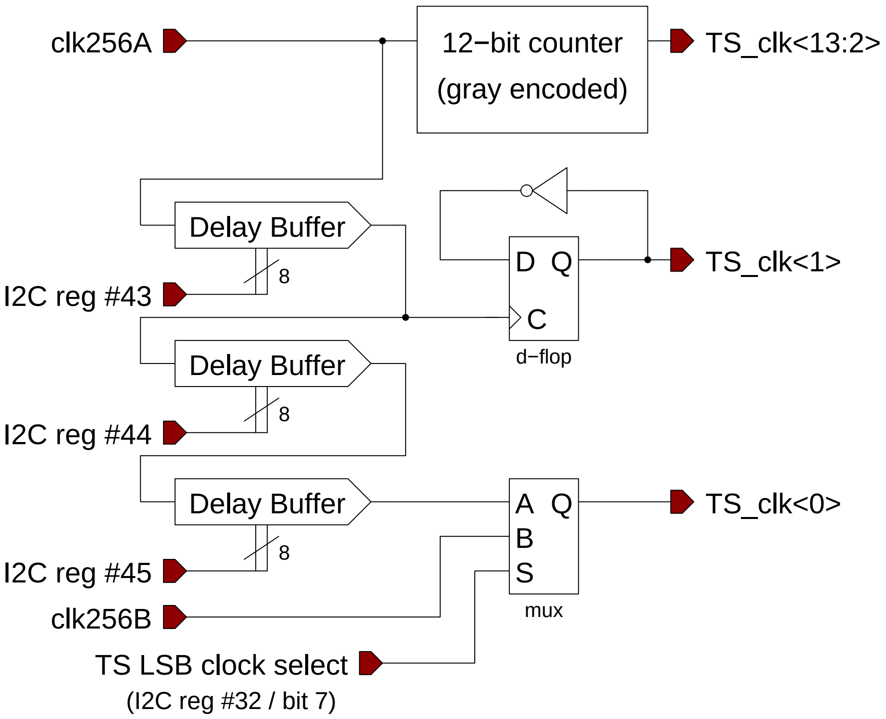


Figure 16: Time-stamp generation principle

will be internally generated (see chapter 4.9). For homogeneous time bining, registers 43 to 45 then need to be adjusted. This should be the normal clock operation mode.

The other, optional mode, was included as a fall back solution in case any circuitry should have resulted faulty. To operate the *n-XYTER* with two, phase shifted input clocks, *clk256A* and *clk256B*, Configuration Register 32, bit 7 needs to be set to 1. In this case, only delay register 43 is relevant. The externally imposed phase shift between *clk256A* and *clk256B* further determines homogeneity of the time stamp.

TS LSB clock select (bit 7 of Configuration Register 32):

- when 0, the LSB of the time stamp is derived from clk256A
- when 1, the LSB of the time stamp is derived from clk256B

The internal structure of the delay buffers is presented in figure 11. The effective delay of the buffer may be programmed by attaching capacitive loads to the outputs of four serially connected inverters. Note that pairs of capacitors are connected serially to optimize minimum delay of the buffer.
The presented configuration allows adjusting of the delays for input *clk256A* clock frequencies from 128 MHz to 256 MHz.

4.9.2 Readout clocks

The *n-XYTER* uses internally generated readout clocks which are accessible from two pairs of LVDS output pins:

- 32 MHz is used in the token ring, the memories and the analogue multiplexer. It is available on an LVDS output.
- 128 MHz is used for data transfer off the chip and is likewise available on an LVDS output.

By default, after reset of the I^{2}C registers, readout clock and data transmission clock are derived directly from *clk256B*. For operation in this setting, *clk256B* should be driven at 128 MHz in order to obtain the normal data transfer frequency. The start-up default is the one operating at lower frequency.
For operation at the nominal frequency of 256 MHz, the clock configuration needs to be modified by setting bit 3 of Configuration Register 33 to 1. This is the normal operation mode!

Readout clock select (bit 3 of Configuration Register 33)

- when 0 (startup setting), the readout clock is obtained by dividing *clk256B* by 4, the data transmission clock *clk128* is the buffered clock *clk256B*.
- when 1 (normal operation mode), the readout clock at 32 MHz and the clock for the digital output buffer (also called transmission clock) at 128 MHz, are obtained by dividing *clk256A* by 8 and by 2 respectively.

5 Data Transfer

Data read out from the local FIFOs through the token ring is then synchronously transferred off the chip. To this end, the analogue data is fed into a dedicated differential readout buffer at the token ring operating rate of 32 MHz, while the digital data gets multiplexed fourfold onto 8 differential LVDS output lines. In this scheme, every data element consists of a 14 bit time-stamp, a six bit channel number and three additional diagnostic bits. The analogue differential output buffer is designed for a differential output impedance of 100 Ohms.

5.1 Digital Output Format and Timing

For each recorded pulse a total of 25 significant bits will be sent off chip.

Data bits are split into 4 8-bit packets, transmitted at 4 times the main clock frequency (i.e. 4 x 31.25 MHz = 125 MHz).

The token is generated when at least one FIFO has data in it (the FIFO has a *empty* signal which trigger the token generation), the token comes out from the token manager circuit and starts to travel in the ring. Once the token arrives at the channel which contains data, it stops and generate a signal *read* to get the data out from the FIFO memory. Then, at the next read out clock cycle, it goes on and stops to the next channel which contains data. If there are no more channels which have data, the token reaches the token manager. When the token manager recognize the condition to restart this procedure (at least one FIFO has data in it) it releases the token again and repeats all the above steps.

When the FIFOs are read, both the analog (pulse amplitude) and digital information (timestamp, channel id, data valid, pile up signal, overflow signal) are sent to the output.

If no data is avaliable from the FIFOs, the Data Valid bit (bit 7 in the first packet) is always 0.

Output is differential LVDS standard.

In some circumstances, the data valid (DV) bit (the bit 7 of the first packet) is not properly set, even if the timestamp is valid and the interal circuits recognize and record the event. The data might reach the output with the the data valid (DV) bit (the bit 7 of the first packet) stucked at 0, all the remainig bits of the 4 packets are indeed valid.

Table 12: Digital Output Format

	7	6	5	4	3	2	1	0
0	**DV** [1]	**TS13**	**TS12**	**TS11**	**TS10**	**TS9**	**TS8**	**TS7**
1	**0**	**TS6**	**TS5**	**TS4**	**TS3**	**TS2**	**TS1**	**TS0**
2	**0**	**ID6**	**ID5**	**ID4**	**ID3**	**ID2**	**ID1**	**ID0**
3	**0**	**0**	**0**	**0**	**0**	**PileUp**	**OverF**	**Parity**

[1] data valid

Table 13: Digital Output Format when no data is avaliable from the channels

	7	6	5	4	3	2	1	0
0	0	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1
2	0	1	1	1	1	1	1	1
3	0	0	0	0	0	1	1	0

Data packets are transferred at the readout clock frequency of nominally 32 MHz. The sequence of four bytes is however not in phase with *clk32MHz* but rather shifted by 180°.

The output packets contain Gray encoded data. To convert from the Gray code format to binary code format the table 18 in Appendix E provides the translation for the time-stamp and table 19 in Appendix E provides the translations for the channel identifier. The circuits in the FPGA might use the suggested circuit shown in figure 18 to decode the time-stamp information and the circuit shown in figure 19 to decode channel ID information.

5.2 Analogue Data Transfer, Timing

For every data element identified by the token ring for data readout, the corresponding local analogue FIFO pulse hight storage cell is connected to the analogue readout bus and fed to the analogue readout buffer. As the token ring

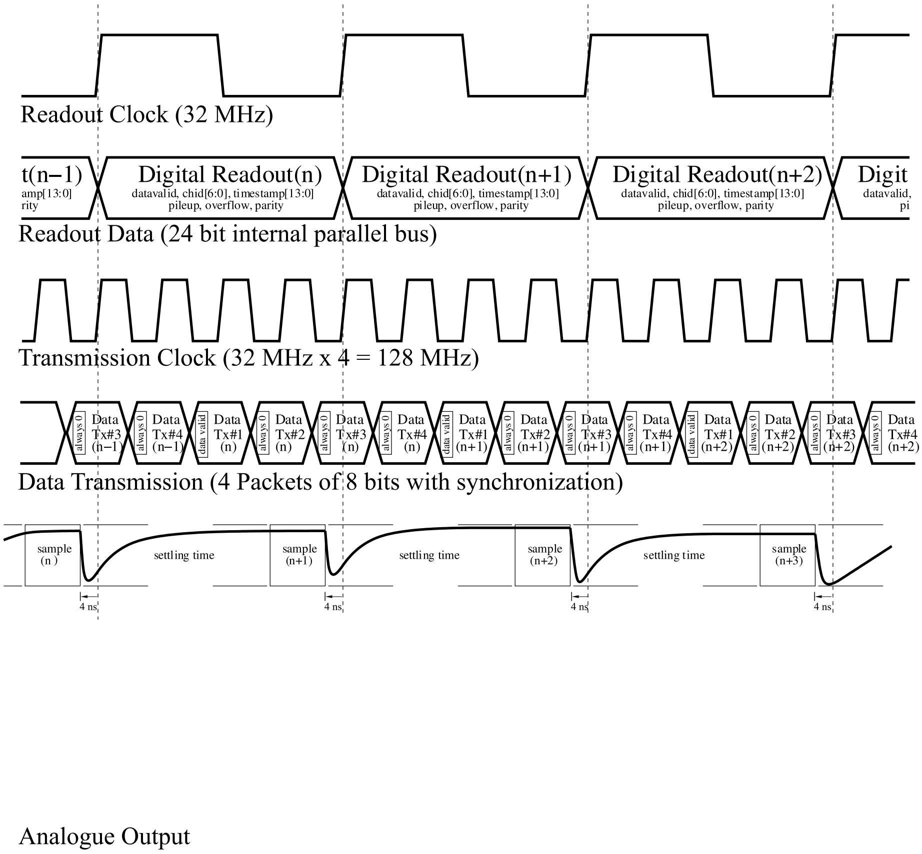


Figure 17: Output data diagram for timing reference. Note that the analogue output data is valid about 4 ns prior to the 32 MHz frame clock. Also, transmitted data is not in phase with the readout clock *clk32MHz* also transmitted.

initiates readout at the frequency of *clk32MHz*, analogue data values are generated at the analogue output buffer at this frequency too as long as there is valid data stored in channel FIFOs. The analogue data chain is designed to cope with this data rate. Nevertheless, the maximum available time should be employed for the signal to settle before readout.
Figure 17 shows the sequence of data as it is transferred off the chip. Note in particular, that corresponding data elements are time shifted. Further more, the analogue signal is to be sampled as late as possible within the data frame as settling of the signal needs to be accounted for. Measurements show that a repeated transfer is initiated yet even before the data frame clock (32 MHz) transits in its positive edge.

The analogue signal is valid 4ns prior to the 32MHz positive clock transition. It should be sampled as late as possible

The sampling point of for the analogue data appears about $\frac{5}{4}$ of a readout frame earlier than the first data element of the digital packet. In practical considerations, the existence of this delay is irrelevant, as any external ADC connected to the analogue data line will introduce its own additional delays, so that energy and timing information will need to be aligned in any case after signal conversion.

Note that after a sequence of data terminates and no further analogue data is read out, the analogue output signal slowly settles to some intermediate level, which reflects the fact that the floating internal analogue data bus discharges to some potential that carries no information. The time constant of discharge appears an order of magnitude larger than the active driving capability.

Table 7: Configuration Register 32 (ɪ2c address: 32)

bit	name	description
0	test pulse enable	when high (logic 1) it enables test pulse signal (strobe) for the calibration block; when low (logic 0) the test pulse signal is not active.
1	test pulse synchronise	when high (logic 1) the test pulse signal (strobe) is internally synchronised with clk256A; when low (logic 0) the test pulse (strobe) goes to the inputs without any synchronization.
2	test pulse polarity	when high (logic 1) the test pulse signal (strobe) polarity is positive; when low (logic 0) the test pulse signal (strobe) polarity is negative.
3	test trigger enable	when high (logic 1) it enables the enables the test trigger signal for mask register; when low (logic 0) it disables the test trigger signal for mask register.
4	test trigger synchronise	when high (logic 1) the the test trigger signal is internally synchronised with clk256A; when low (logic 0) the test trigger signal goes to the inputs without any synchronization.
5	disable 32 MHz clk	when high (logic 1) the 32 MHz readout clock is disabled; when low (logic 0) the the 32 MHz readout clock is enabled.
6	disable 128 MHz clk	when high (logic 1) the 128 MHz readout clock is disabled; when low (logic 0) the the 128 MHz readout clock is enabled.
7	TS LSB clock select	when high (logic 1) the LSB of the time stamp the LSB of the time stamp is derived from clk256B; when low (logic level 0) is derived from clk256A.

Table 8: Configuration Register 33 (i2c address: 33)

bit	name	description
1-0	calibration select	2-bit number selecting the set of channels to which the calibration pulse is applied: 00 - tested channels are: 0,4,8,...,124 01 - tested channels are: 1,5,9,. . . ,125 10 - tested channels are: 2,6,10,. . . ,126 11 - tested channels are: 3,7,11,. . . ,127 Note: the test pulse can also be filtered for particular channels by setting bits to 1 in mask register
2	front-end polarity	when high (logic 1) sets front-end polarity to positive; when low (logic 0) sets front-end polarity to negative;
3	readout clock select	when high (logic 1) the 32 Mhz readout clocks are derived from clk256A input: • clk128 is clk256A divided by 2, • clk 32 is clk256 divided by 8 when low (logic 0) the 32 MHz and 128 MHz readout clocks are derived from the clk256B input: • clk128 is buffered clk256B, • clk32 is clk256 divided by 4,
7-4	spare	these bits are reserved for future use and they are not internally connected to any circuit neither or related with the chip functionalty

Table 9: Adaptation of the front-end to different polarities of input signals. Note that VbiasS2 has little influence. The slow shaper output is dominated by the dc level of the first stageŠs output.

I^2Ccontrol register	node manipulated primary	node manipulated secondary	target value positive input charge	target value negative input charge
Vbfb	Vbfb	pre-amp feedback	0.9 V	1.2 V
VbiasF	VcommonF	fast shaper output	1.2 V - 1.5 V	0.5 V
VbiasS	VcommonS	slow shaper output	0.5 V	0.5 V
VbiasS2	VcommonS2	slow shaper output	0.5 V	0.5 V

Table 10: Setting the control bits in the registers to control the delay buffer

Bit No	Output Load Capacitor [pF]	Falling Output [ns]	Rising Output [ns]	Average [ns]
bit 0	10	20.01	17.31	18.71
bit 1	10	20.01	17.31	18.71
bit 2	20	40.01	34.41	37.31
bit 3	60	120.01	102.81	111.71
bit 4	60	120.01	102.81	111.71
bit 5	60	120.01	102.81	111.71
bit 6	60	120.01	102.81	111.71
bit 7	60	120.01	102.81	111.71

Table 11: Clock generation modes

readout_clock_select bit (register number 33, bit 3)	readout clock (32 MHz clock)	times-tamp clock (128 MHz clock)
set to logic level 0 (low), (default)	clk256B divided by 4	clk256B
set to logic level 1 (high)	clk256A divided by 8	clk256A divided by 2

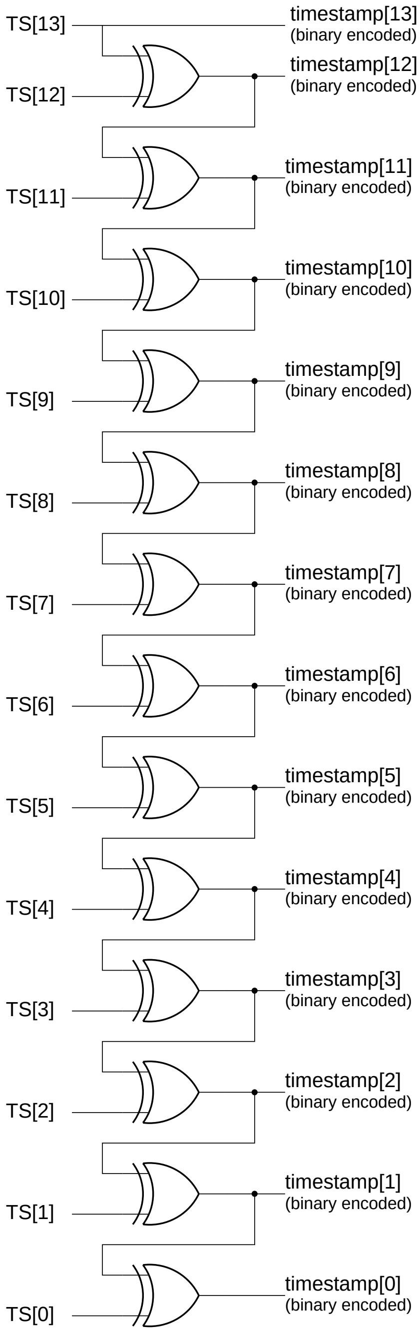


Figure 18: Suggested circuit to convert the time-stamp from Gray-code to binary-code

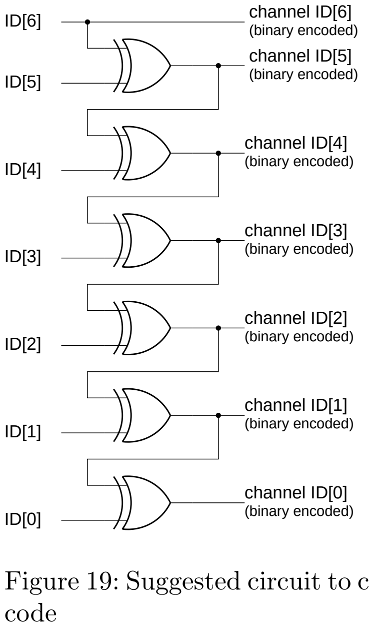


Figure 19: Suggested circuit to convert the channel ID from Gray-code to binary-code

6 Known Problems and Limitations

6.1 Cadence database information

original path : /kip/home1/brogna/PROJECTS/DETNI/RUN2 submitted design : library DETNI2 ; cell HD_NXYTER10 ; view layout actual top cell : library DETNI2 ; cell DETNI2_pads ; view layout/schematic (HD_NXYTER10 is DETNI2_pads plus names, logo, date and markers) process : s35d4 (AMS0.35 SiGe) - HitKit 3.60

Key simulation results are included for test_channel and test_chanblock (see directory Sim_data inside DETNI2/test_channel and DETNI2/test_chanblock).

6.2 Things to be included/ done in the next version of *n-XYTER*

- Retriggerable monostable
- fill empty spaces with capacitors
- replace XOR port with OR in token bypass
- (the XOR port appears to generate a glitch in the token output fom the 16 channels block)
- (the XOR port is in library DETNI2_readout, cell token bypass, instance I4; the layout is in: library DETNI2_readout, cell tkring16; see comment in tkring16-schematic)
- add Uref pad instead of REFM for DACs reference
- Ext_Token_out should be permanently active for monitoring token travel
- 5 V compatible I^2C pads
- ı2c reset should be made asynchronous, due to clk-divider reset!
- Register 42 auto-increment functions should be adapted to n-XYTER needs. Current auto-increment stop to be deleted.
- Add a register to change the duty cycle of bit 0 in the time stamp.
- Make the test trigger input pad a differential LVDS input.
- make delay registers more symmetric
- locate delay reg. 44 just in series with delay register 43, not with register 45.
- define Vreset on chip and tie it to local channel ground
- variable pole zero desired for adaptation to detector applications
- symmetric local thresholds will allow to scan the noise even without input signals
- change the output buffer output stage to a push-pull with less power needs.

A Frontend Schematics

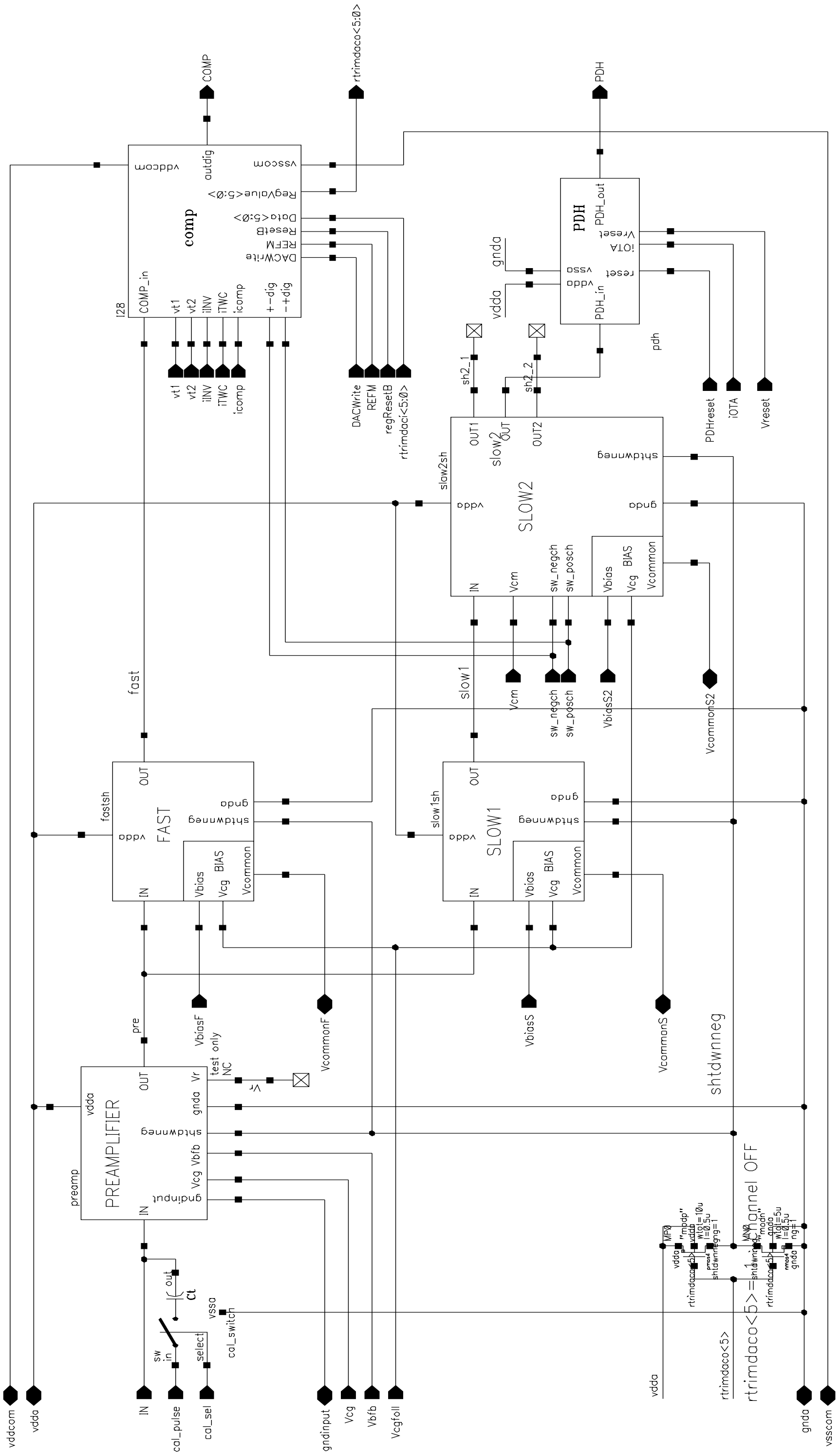


Figure 20: *n-XYTER* front-end schematic; cellname: frontend

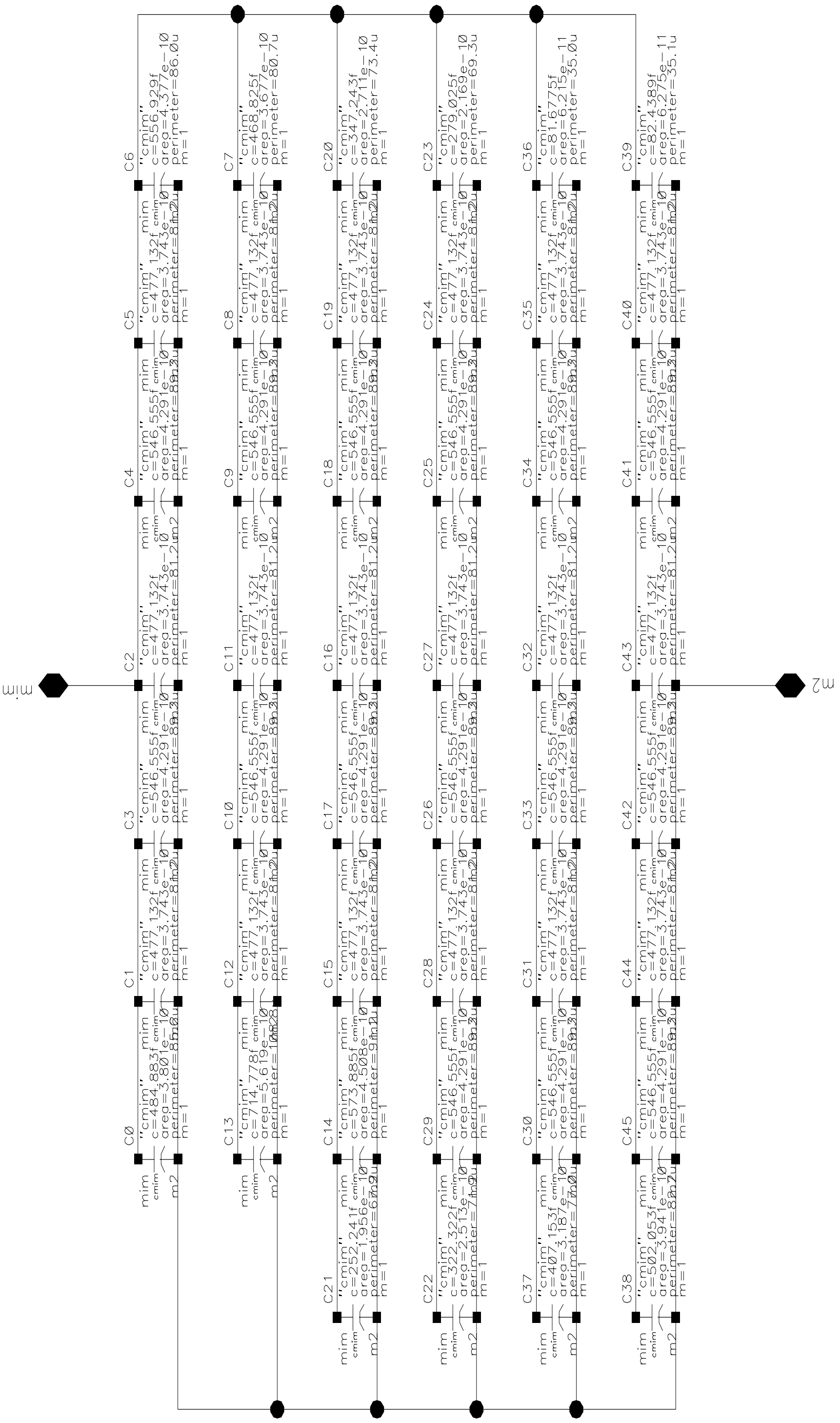


Figure 21: *n-XYTER* front-end schematic; cellname: PRE_MIMCAP45

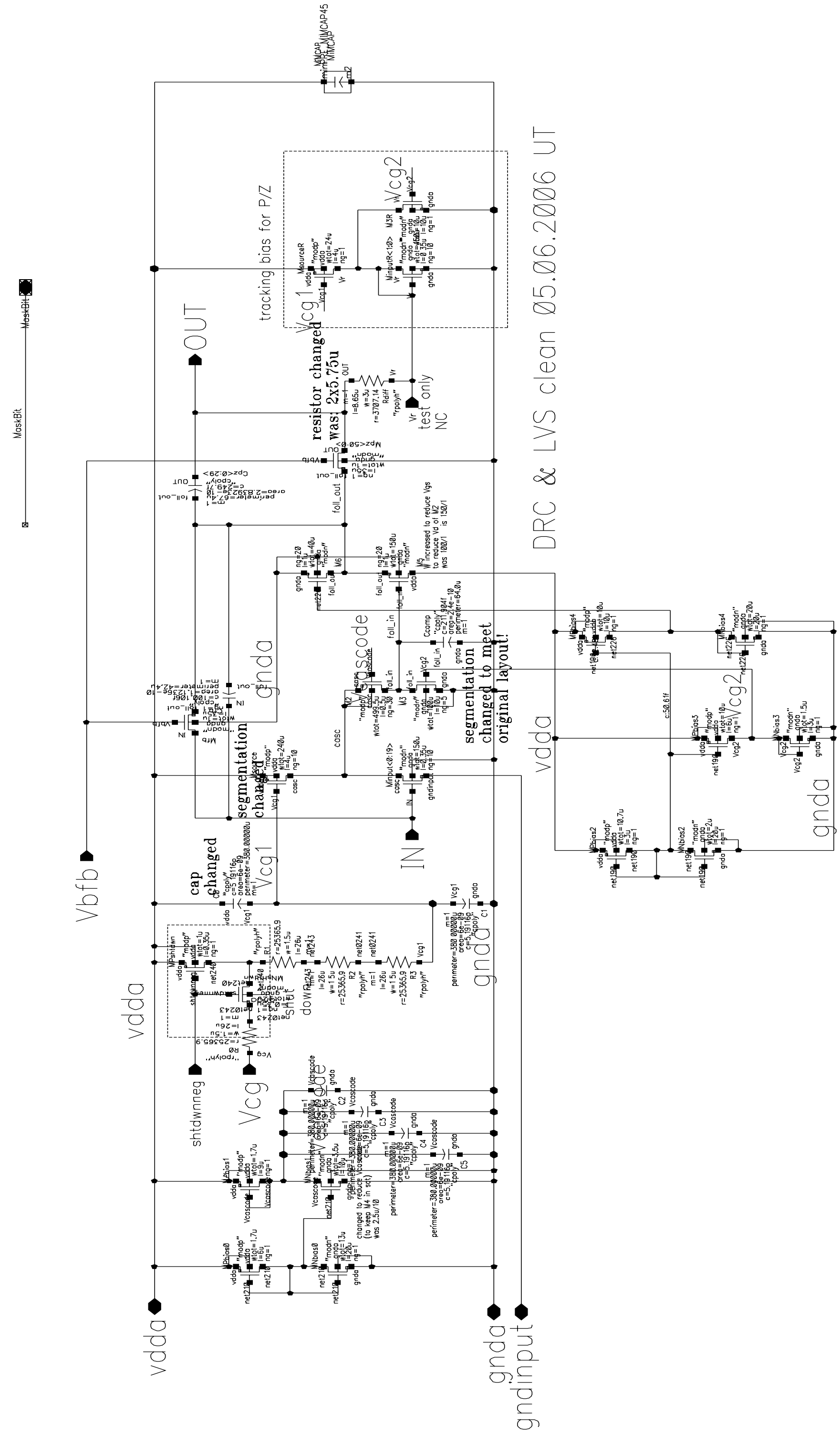


Figure 22: *n-XYTER* front-end schematic; cellname: PREAMPLIFIER

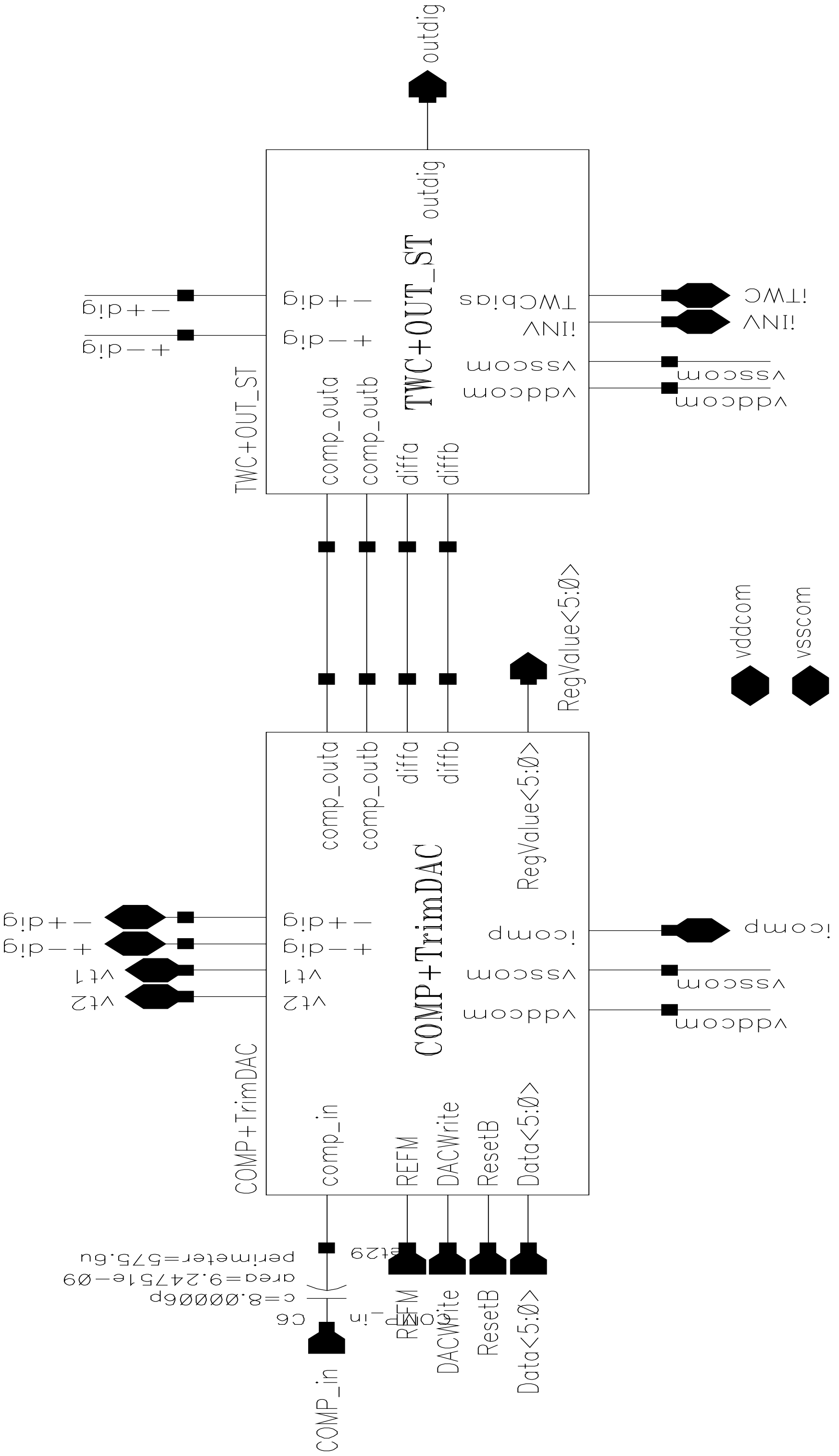


Figure 23: *n-XYTER* front-end schematic; cellname: comp

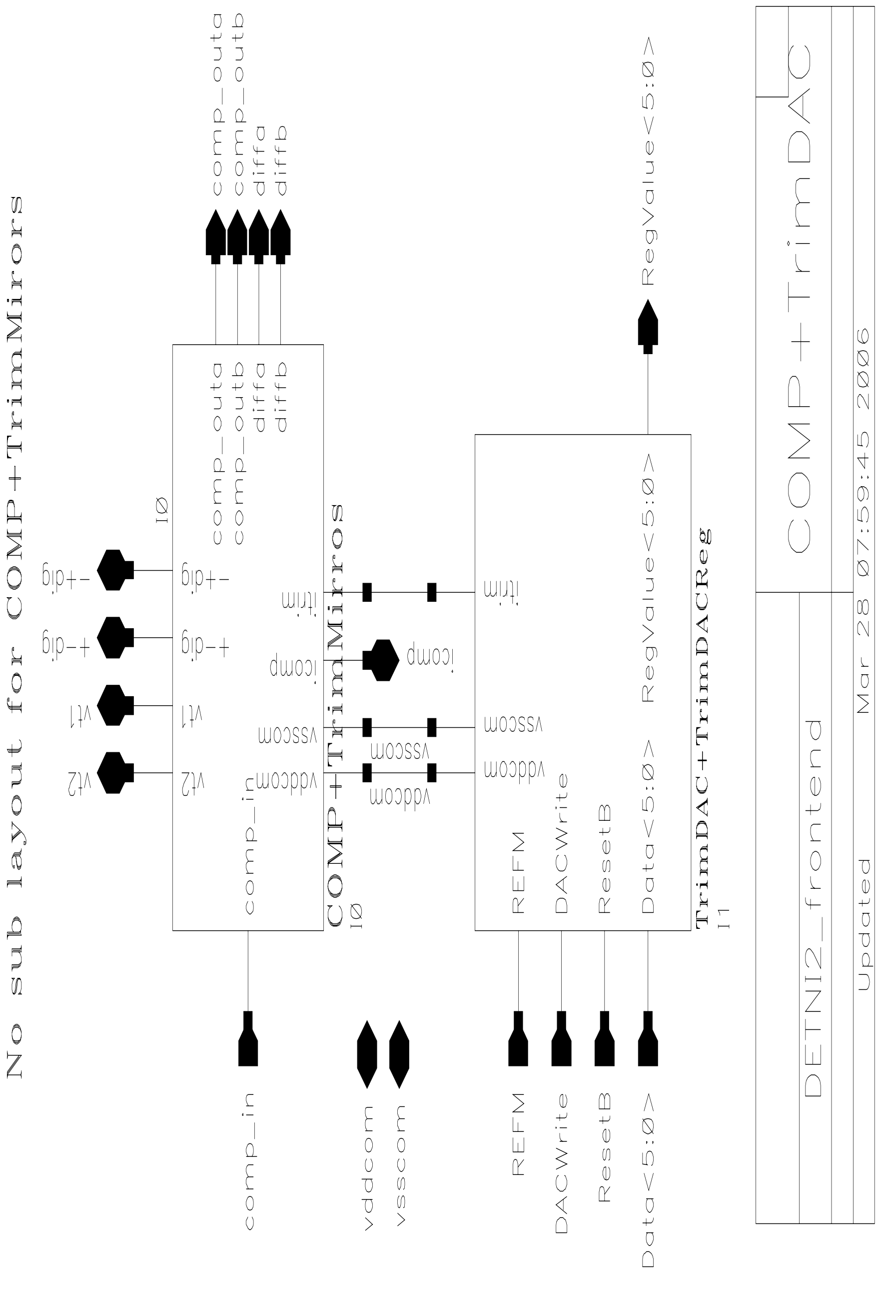


Figure 24: *n-XYTER* front-end schematic; cellname: COMP+TrimDAC

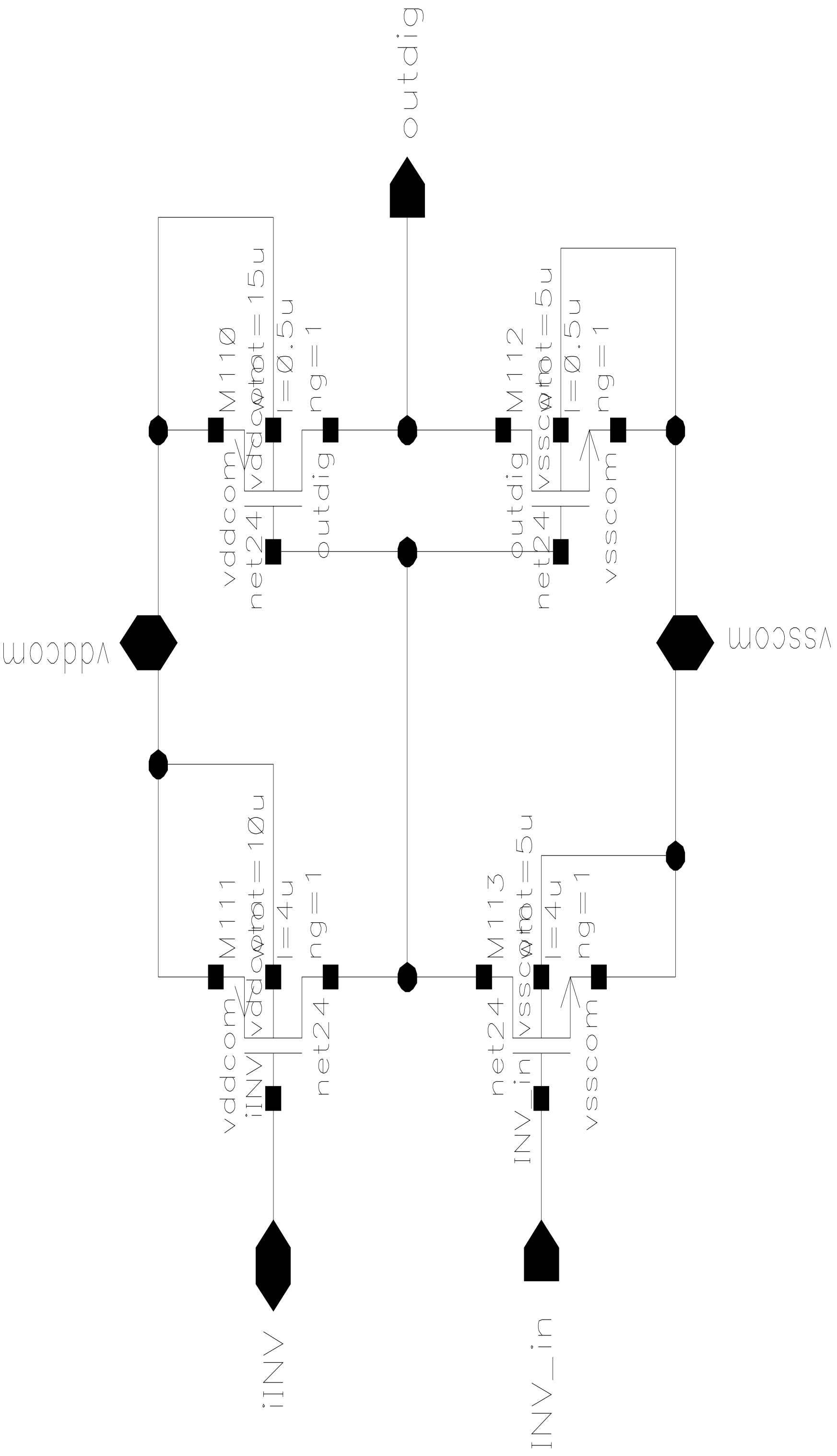


Figure 25: *n-XYTER* front-end schematic; cellname: OUT_ST

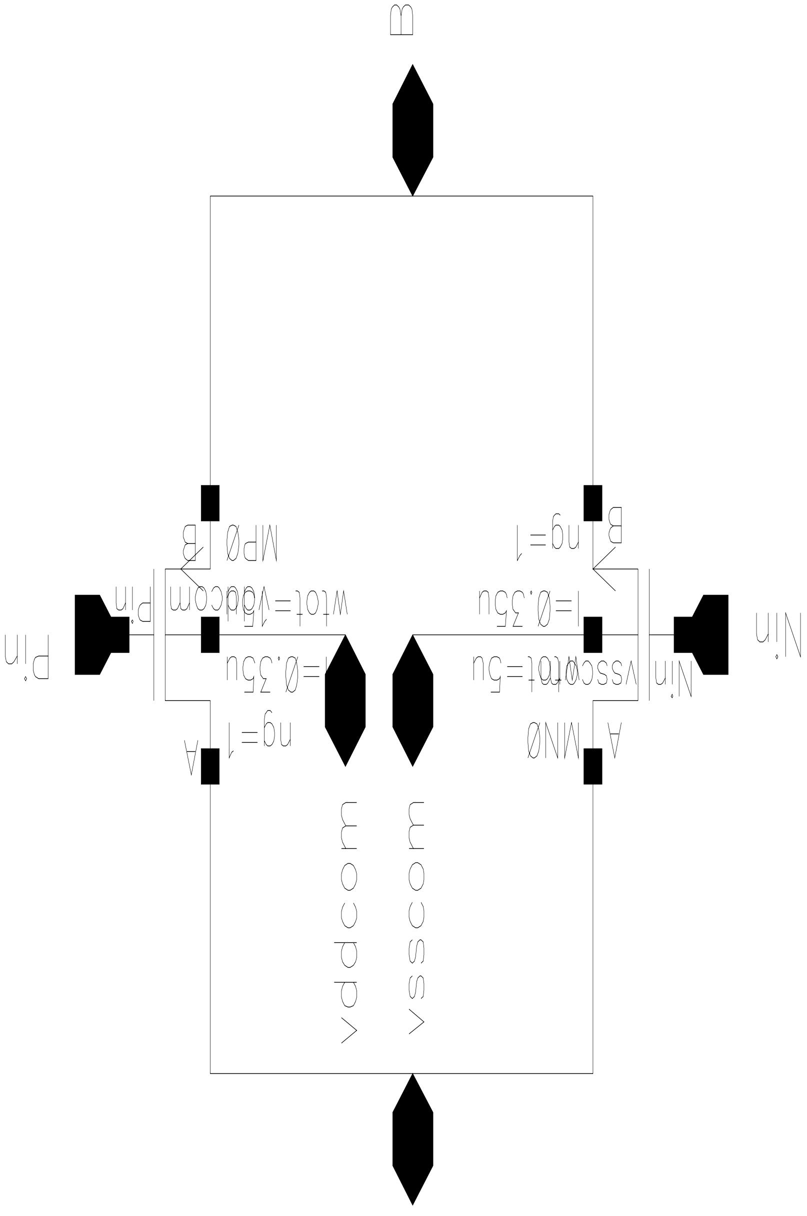


Figure 26: *n-XYTER* front-end schematic; cellname: TG_TWC

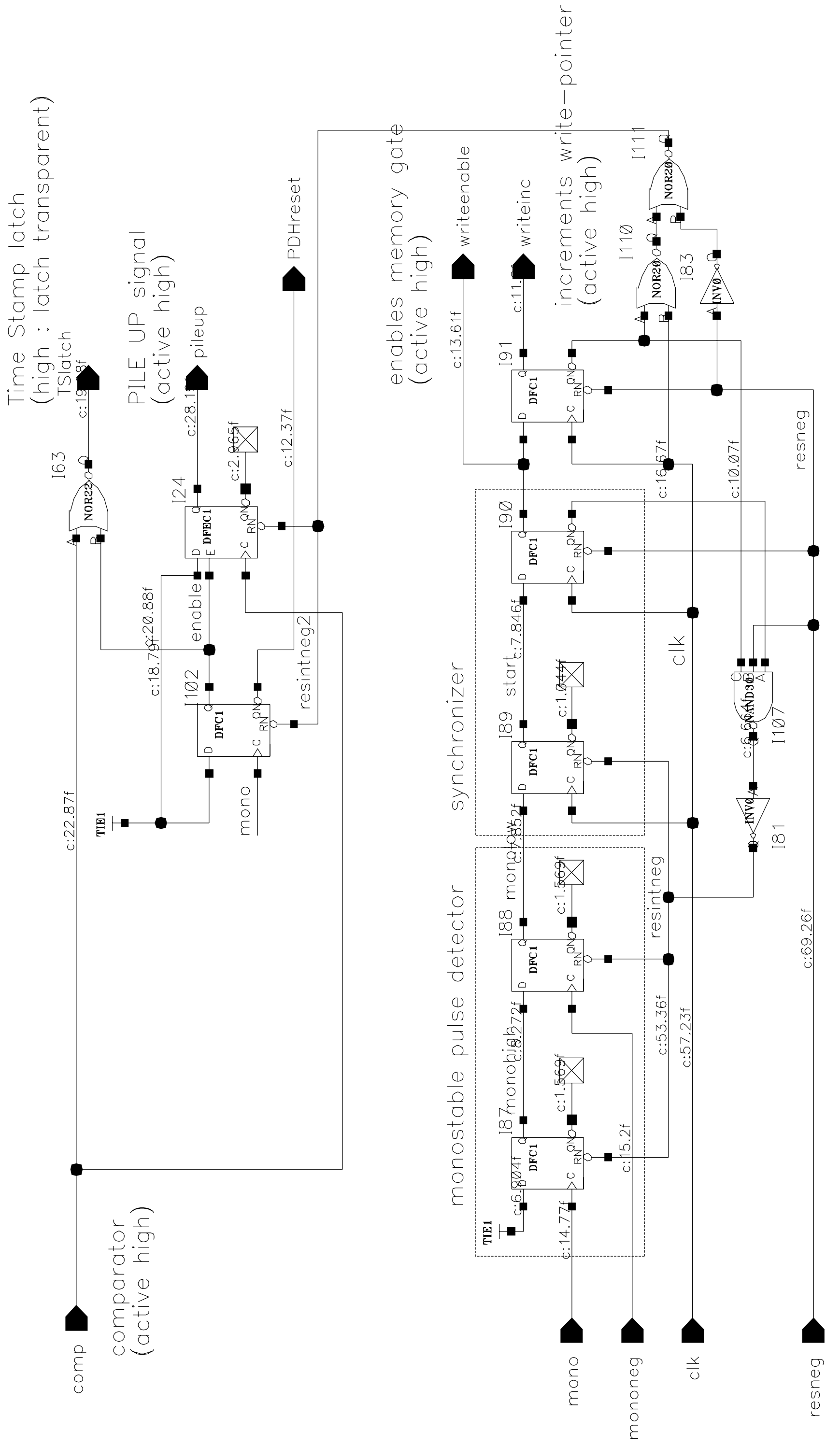


Figure 27: *n-XYTER* front-end schematic; cellname: synchronizer

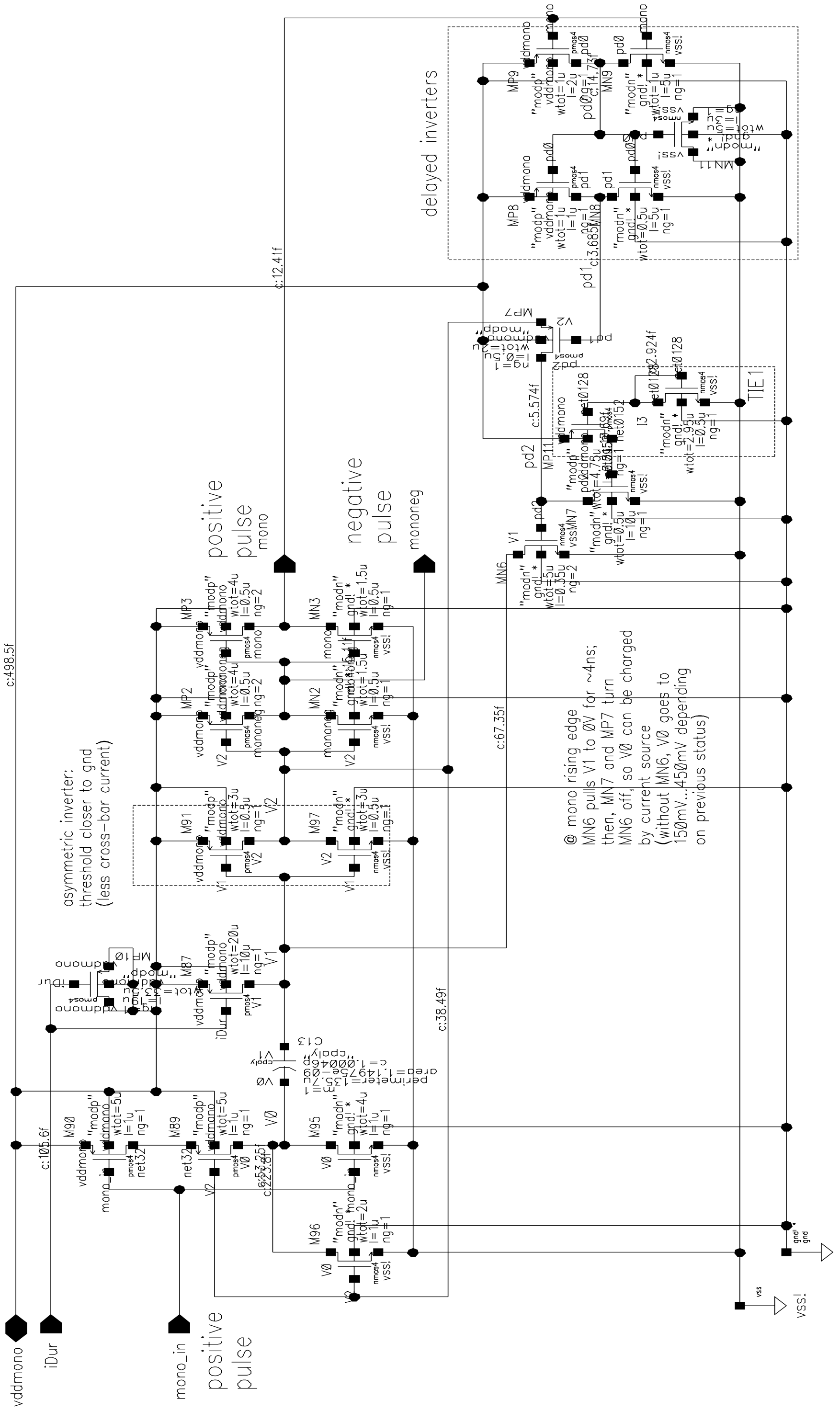


Figure 28: *n-XYTER* front-end schematic; cellname: mono-stable

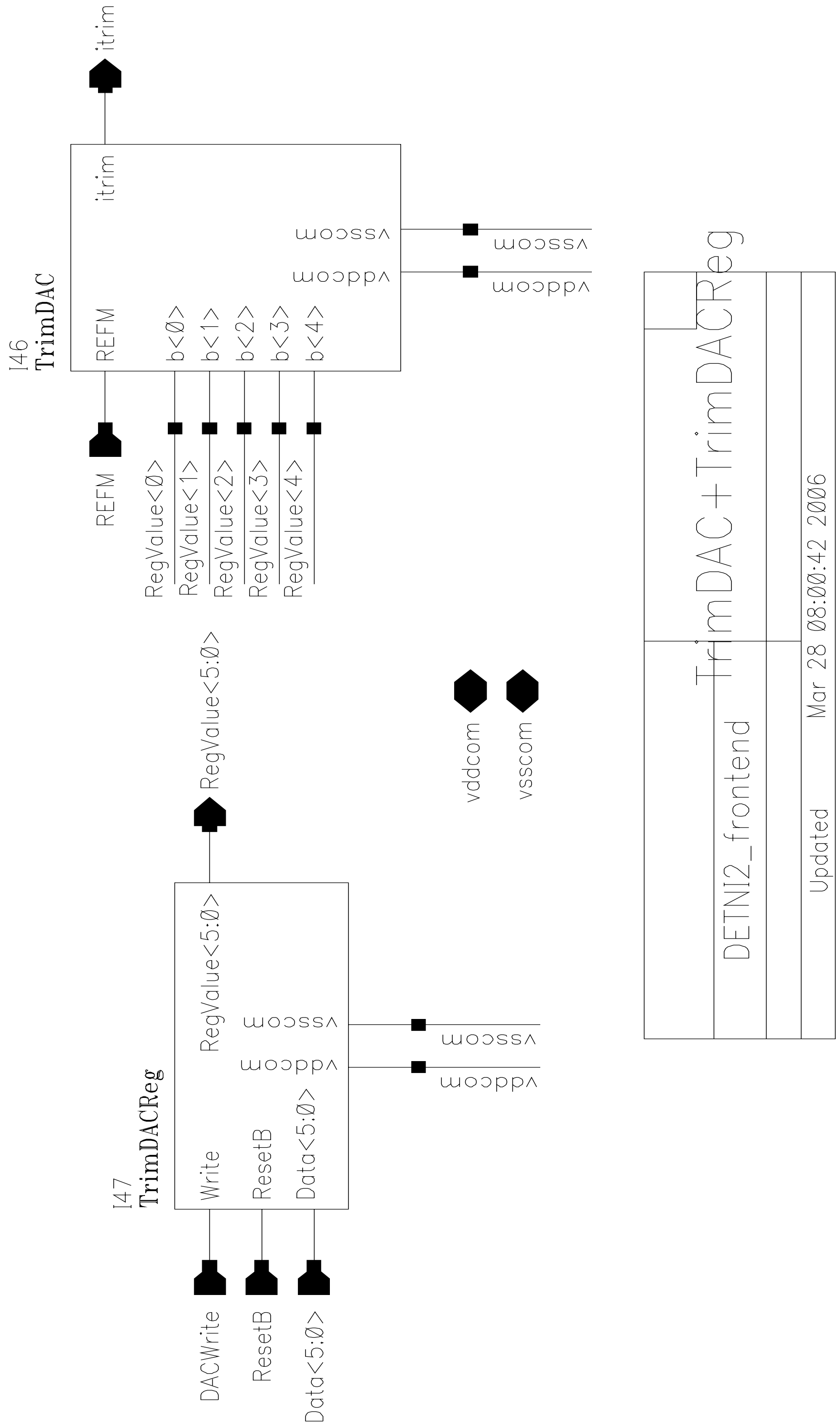


Figure 29: *n-XYTER* front-end schematic; cellname: TrimDAC+TrimDACReg

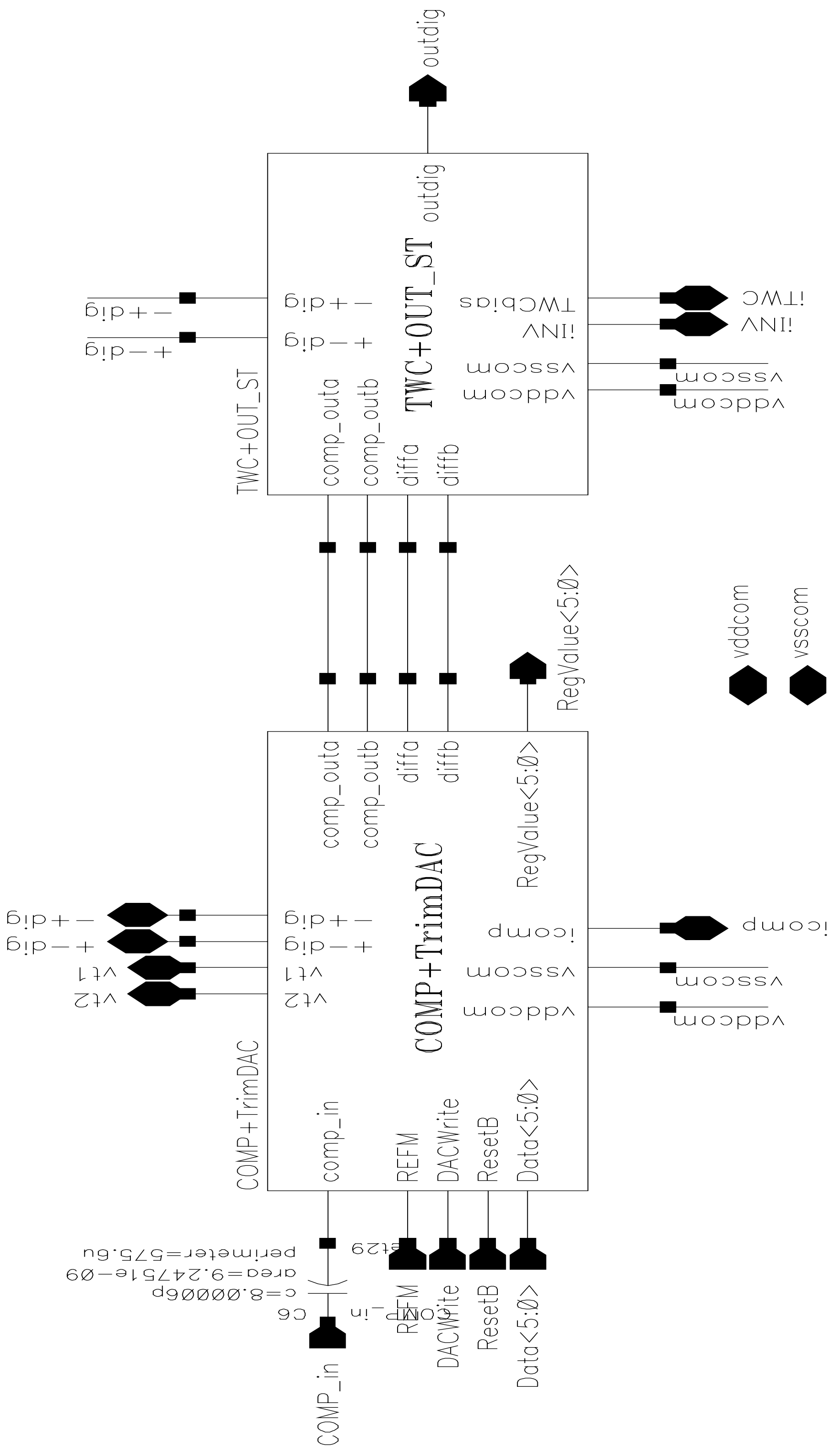


Figure 30: *n-XYTER* front-end schematic; cellname: comp

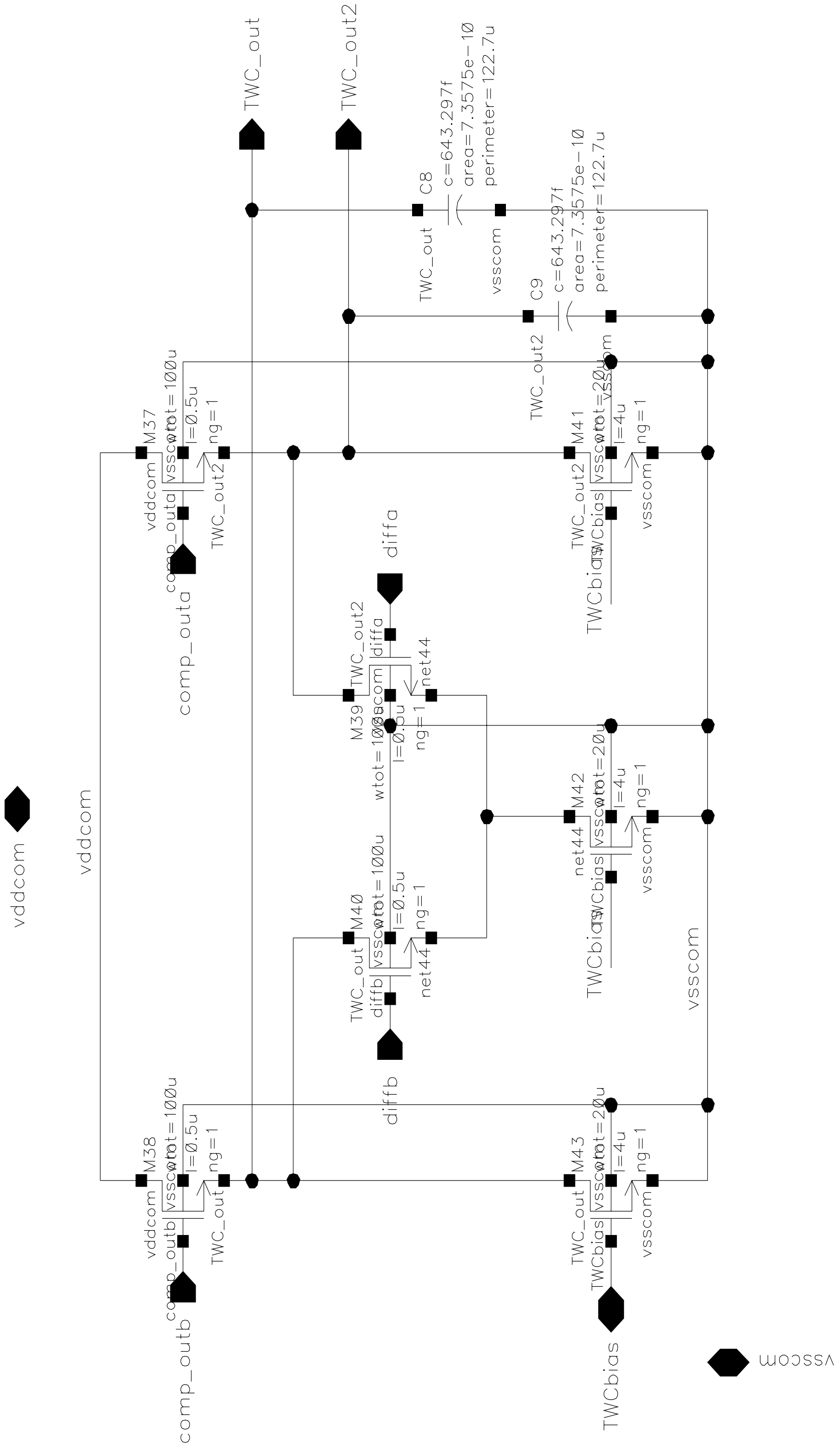


Figure 31: *n-XYTER* front-end schematic; cellname: TWC_var

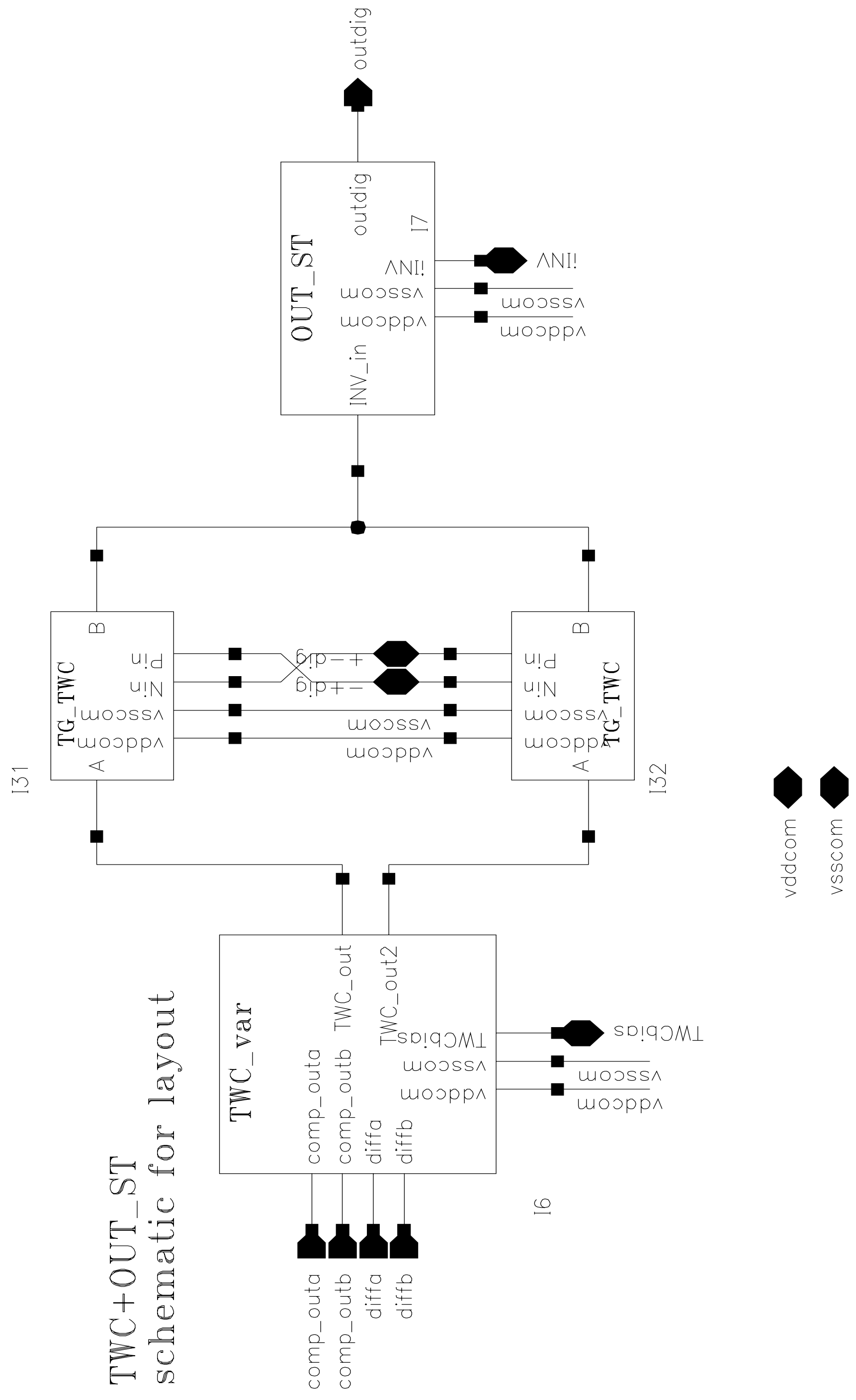


Figure 32: *n-XYTER* front-end schematic; cellname: TWC+OUT_ST

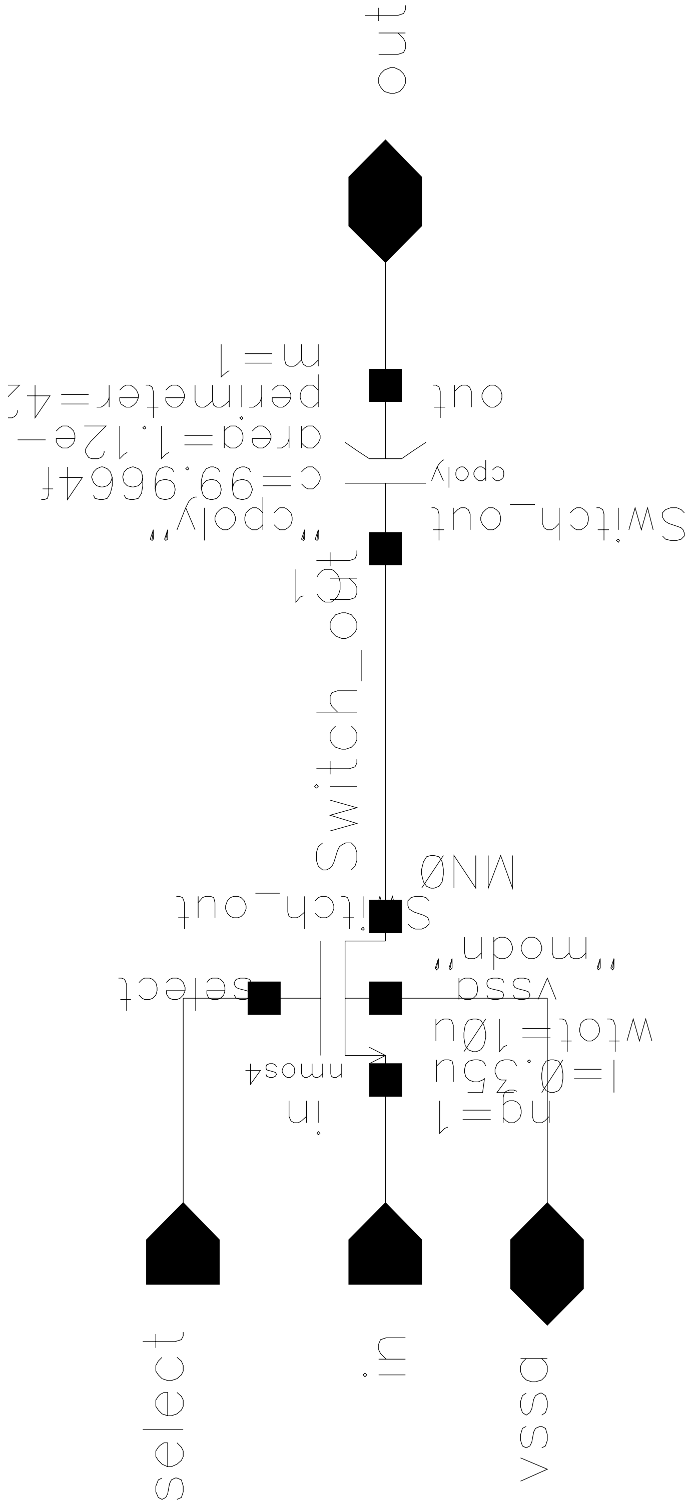


Figure 33: *n-XYTER* front-end schematic; cellname: cal_switch

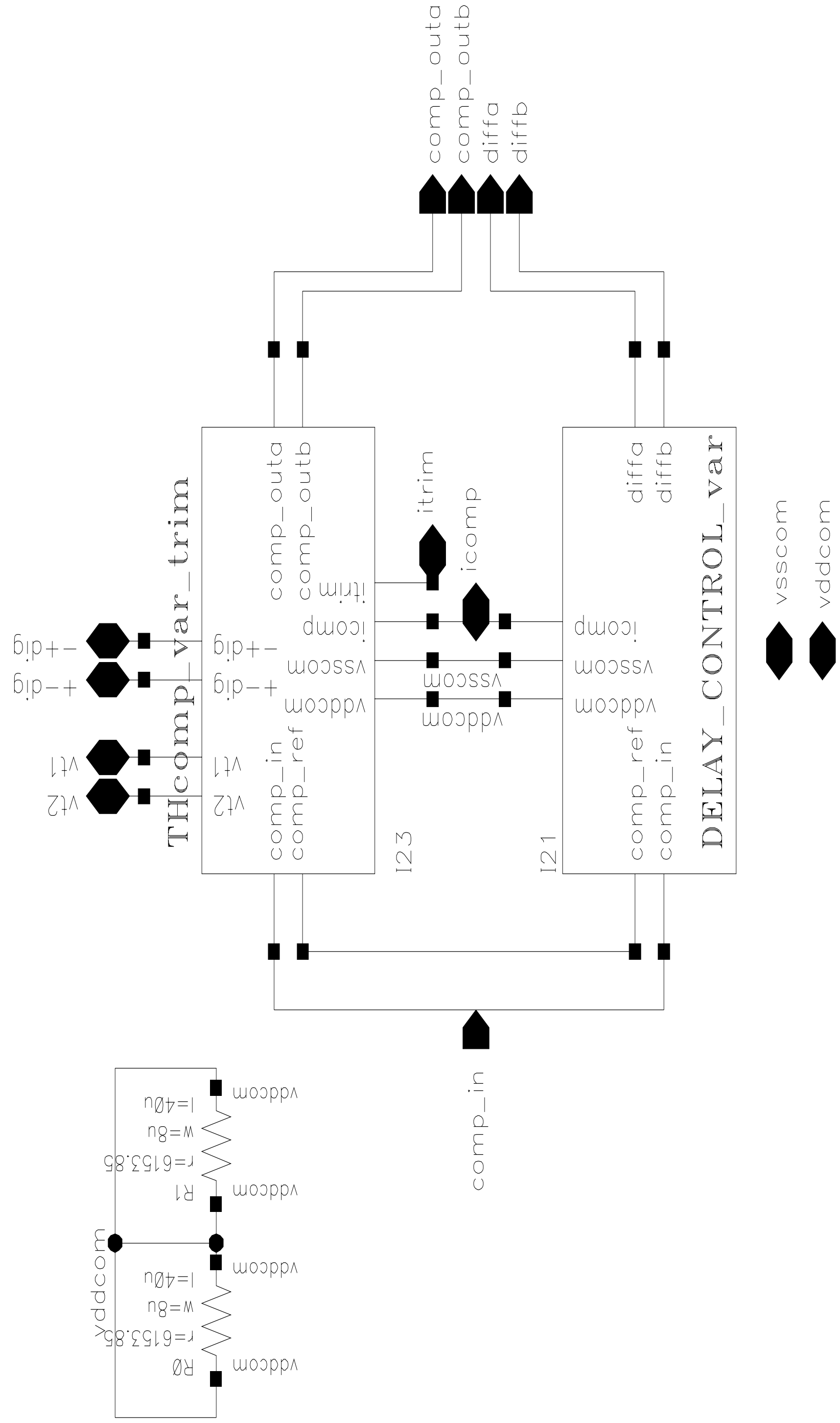


Figure 34: *n-XYTER* front-end schematic; cellname: COMP+TrimMirros

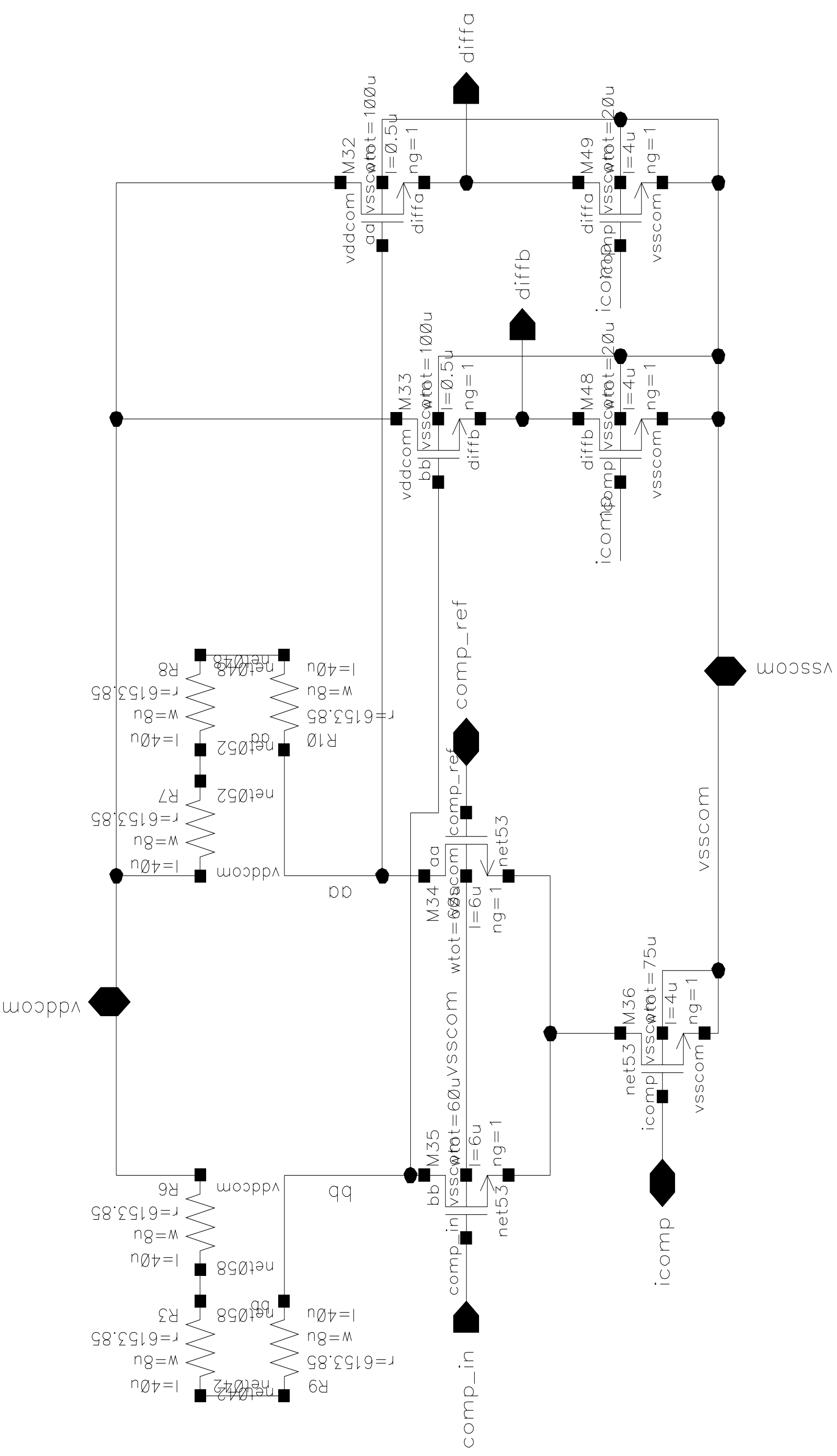


Figure 35: *n-XYTER* front-end schematic; cellname: DELAY_CONTROL_var

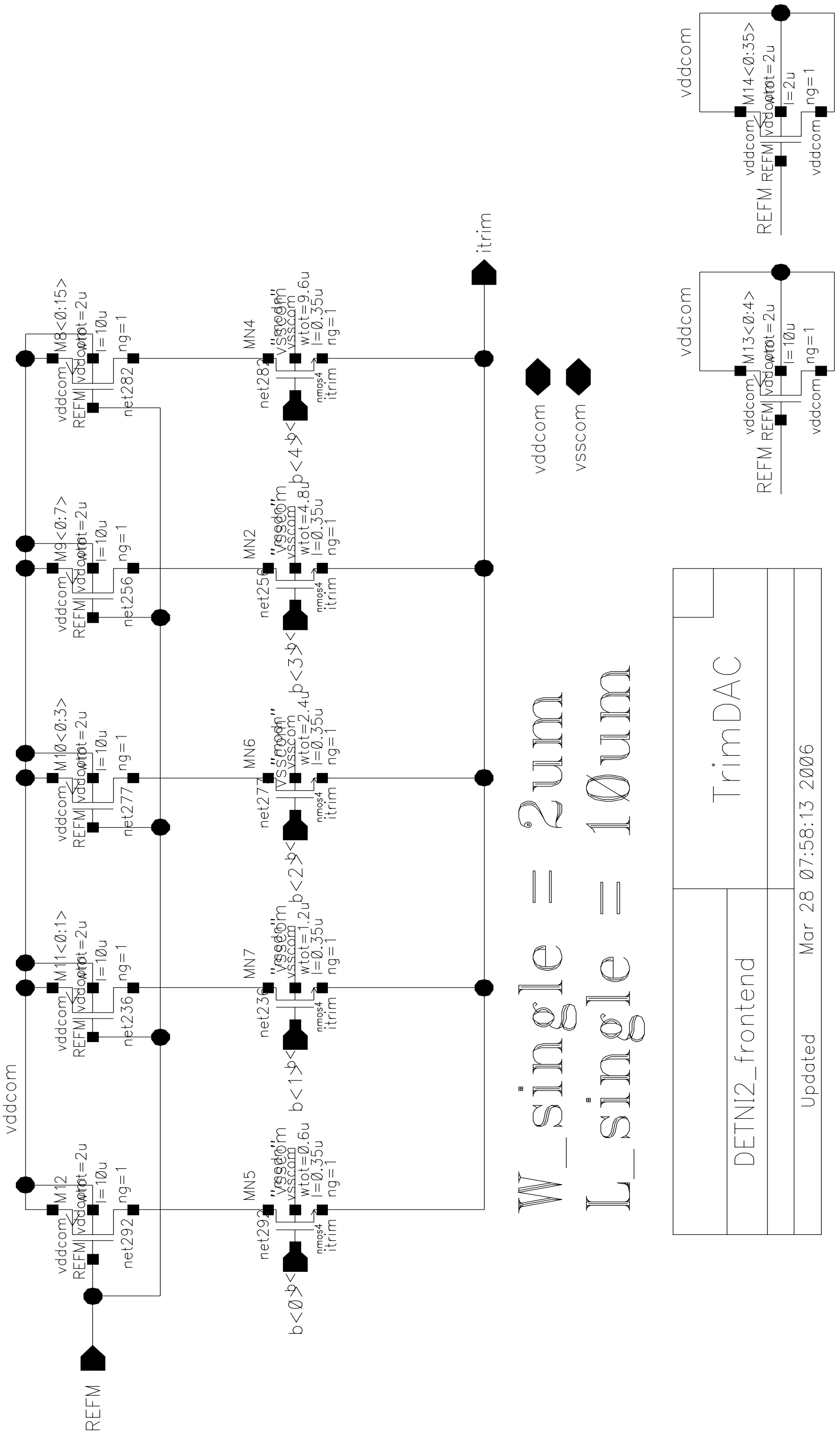


Figure 36: *n-XYTER* front-end schematic; cellname: TrimDAC

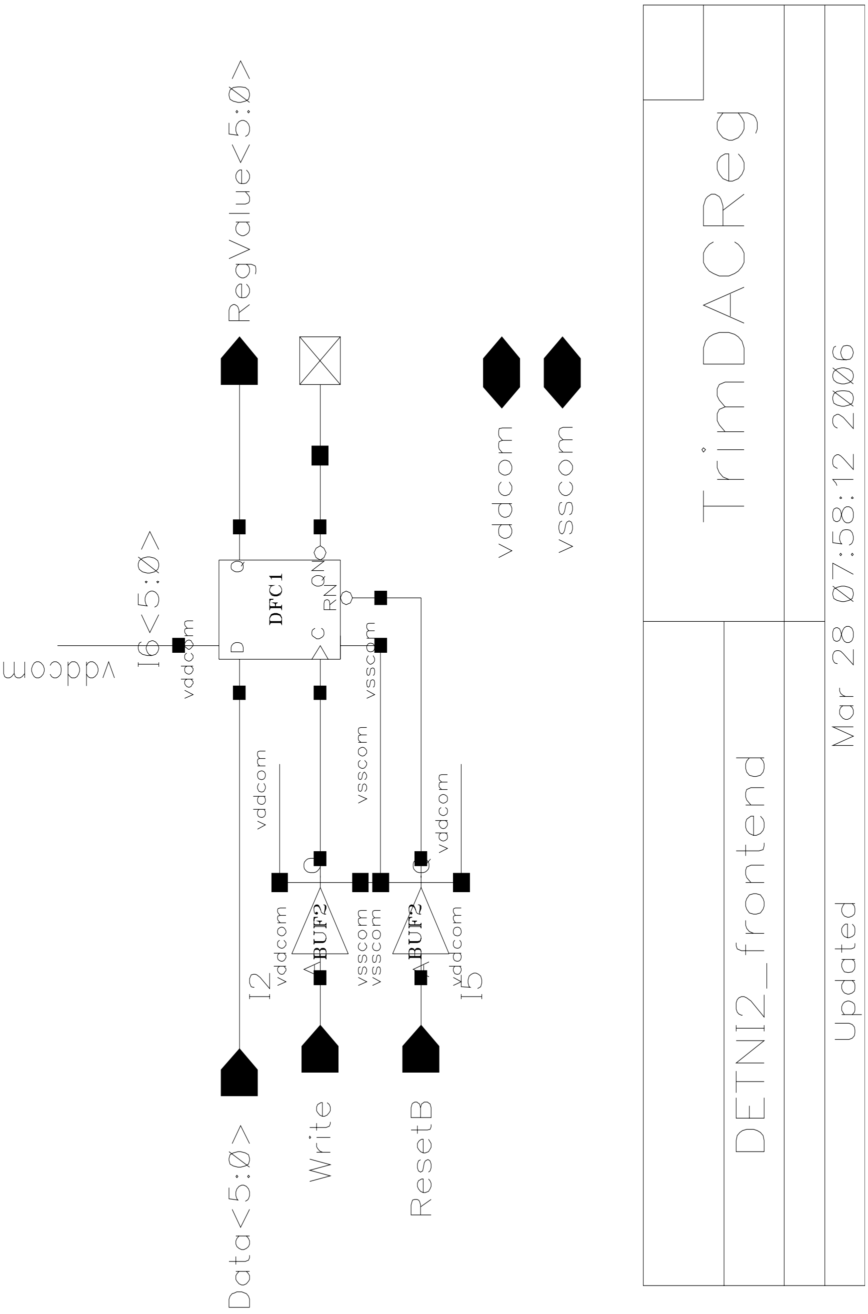


Figure 37: *n-XYTER* front-end schematic; cellname: TrimDACReg

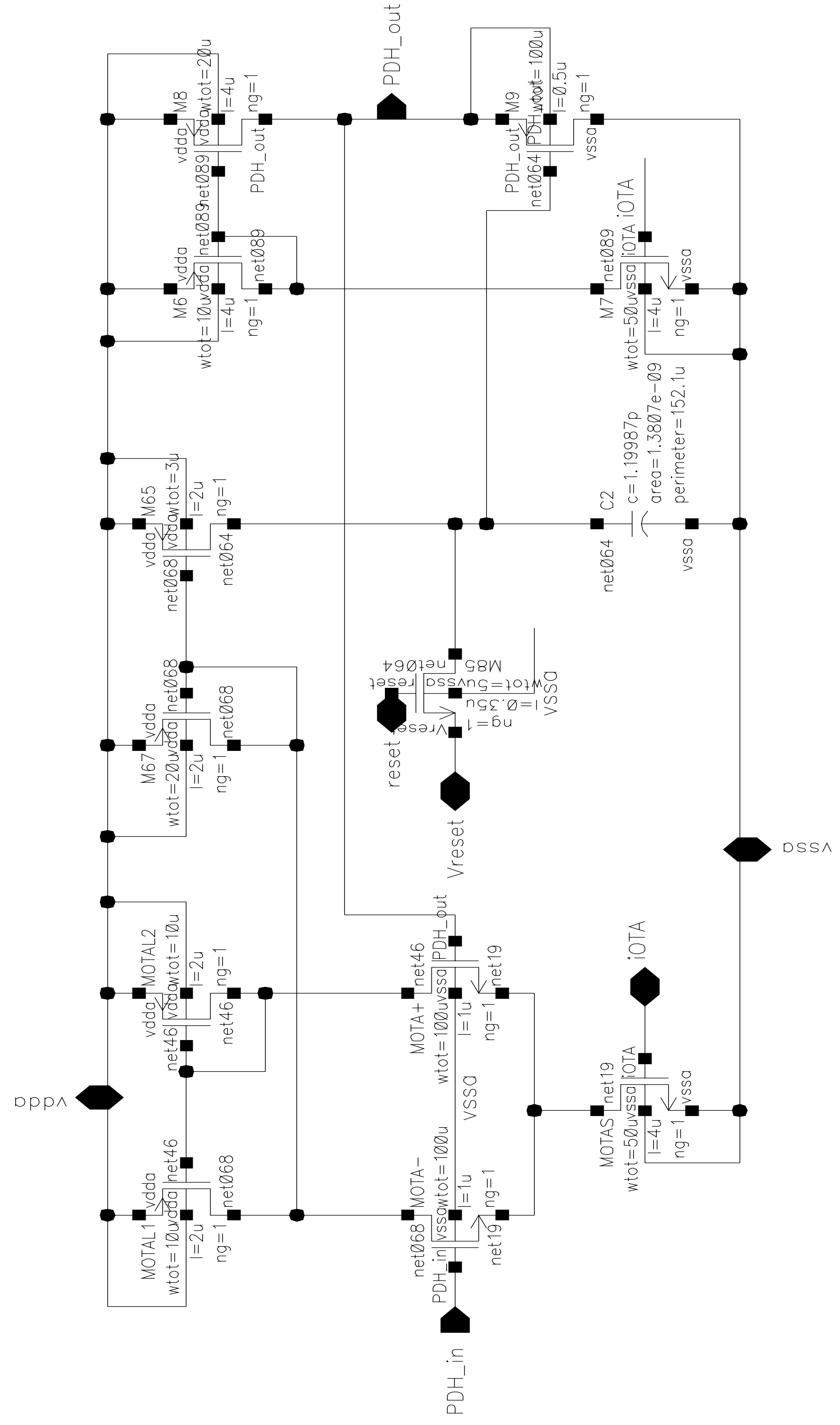


Figure 38: *n-XYTER* front-end schematic; cellname: PDH

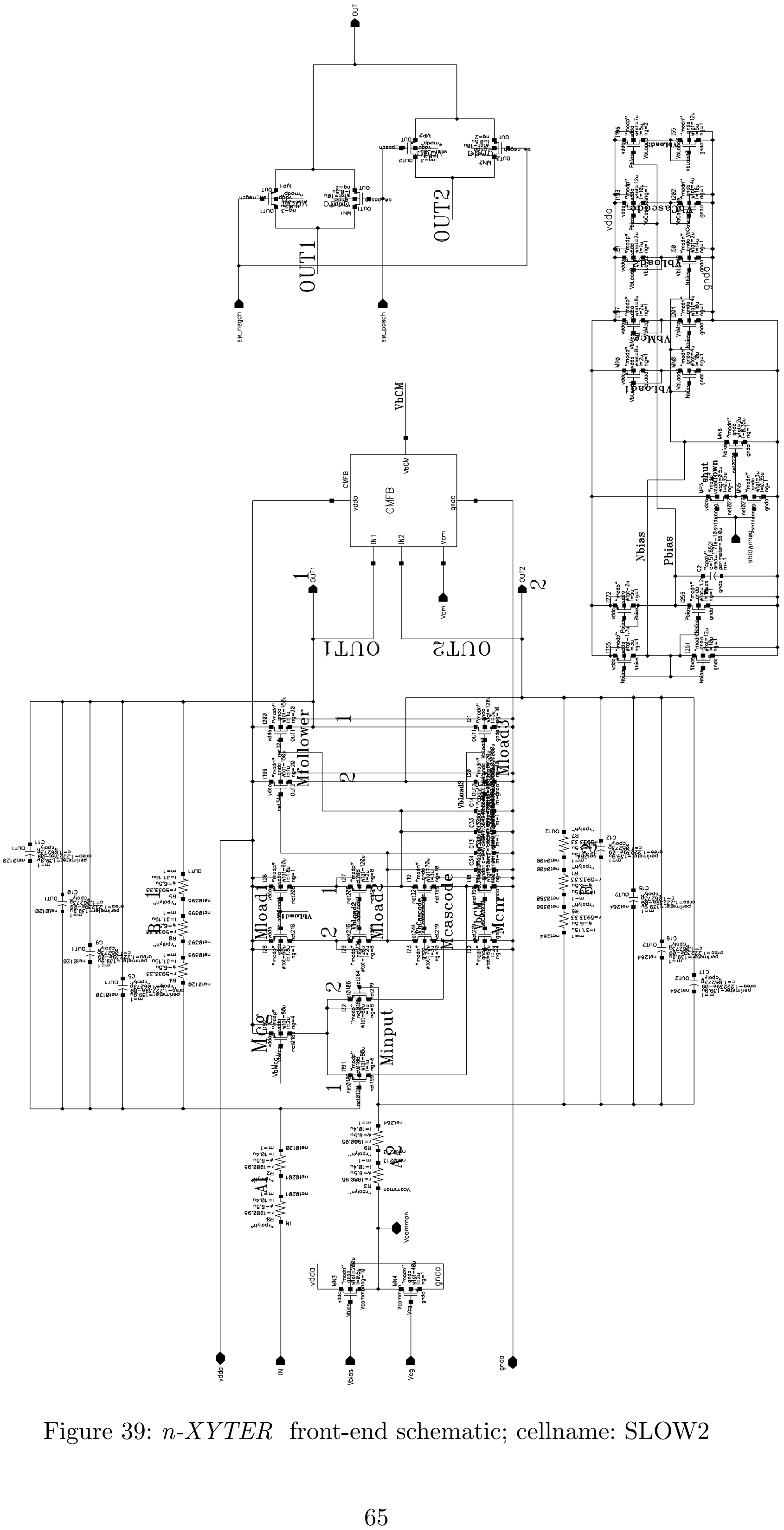


Figure 39: *n-XYTER* front-end schematic; cellname: SLOW2

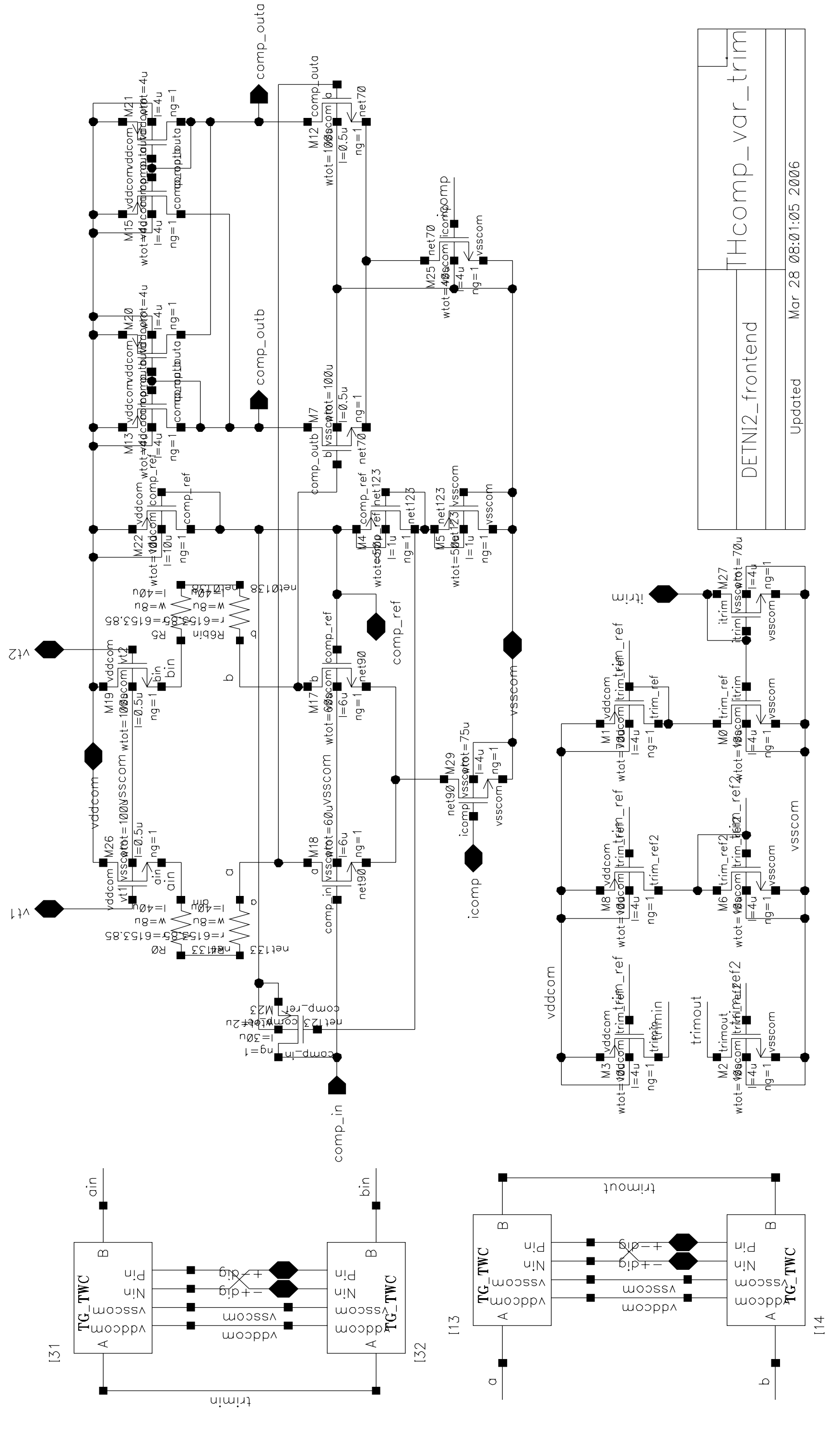


Figure 40: *n-XYTER* front-end schematic; cellname: THcomp_var_trim

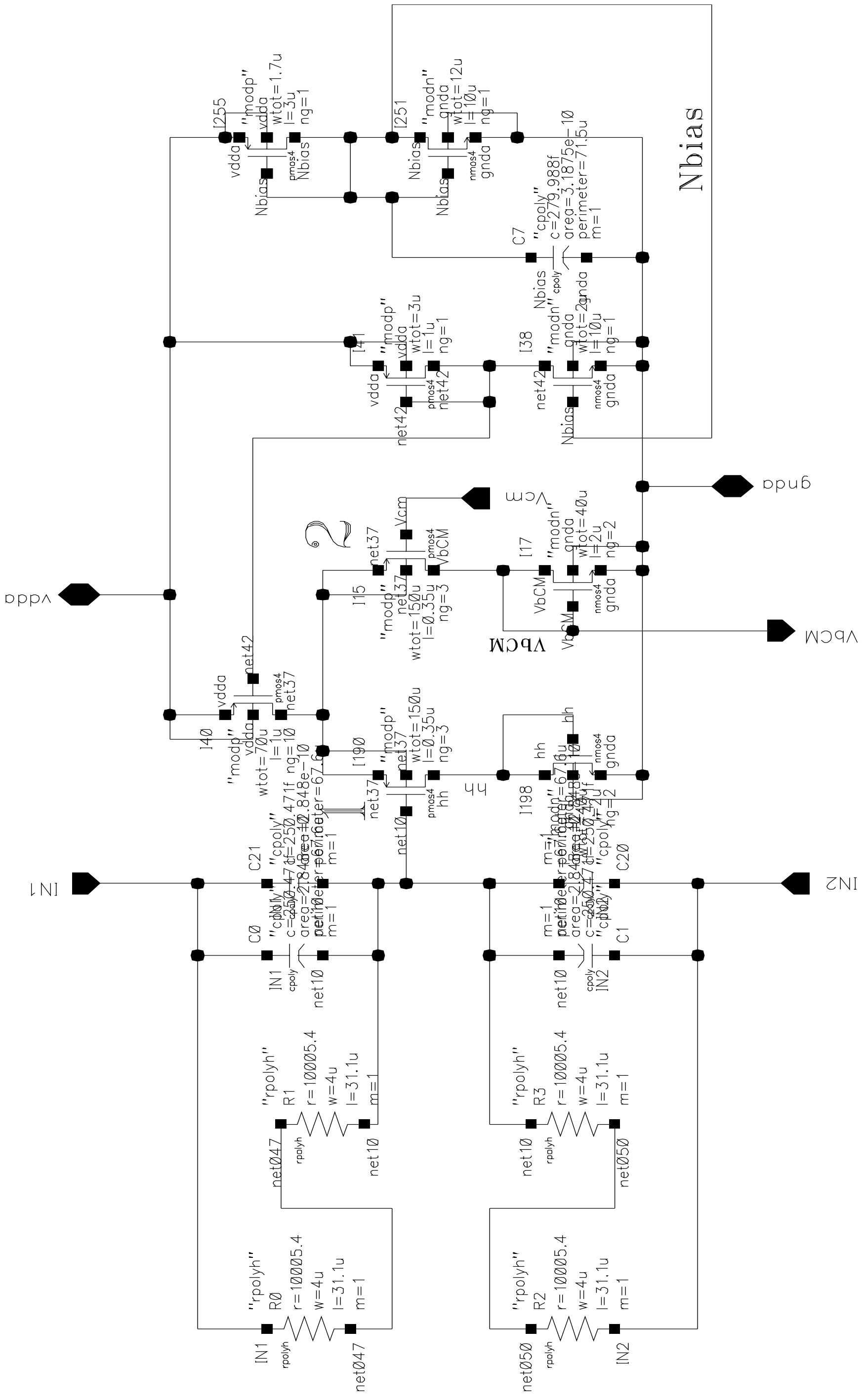


Figure 41: *n-XYTER* front-end schematic; cellname: CMFB

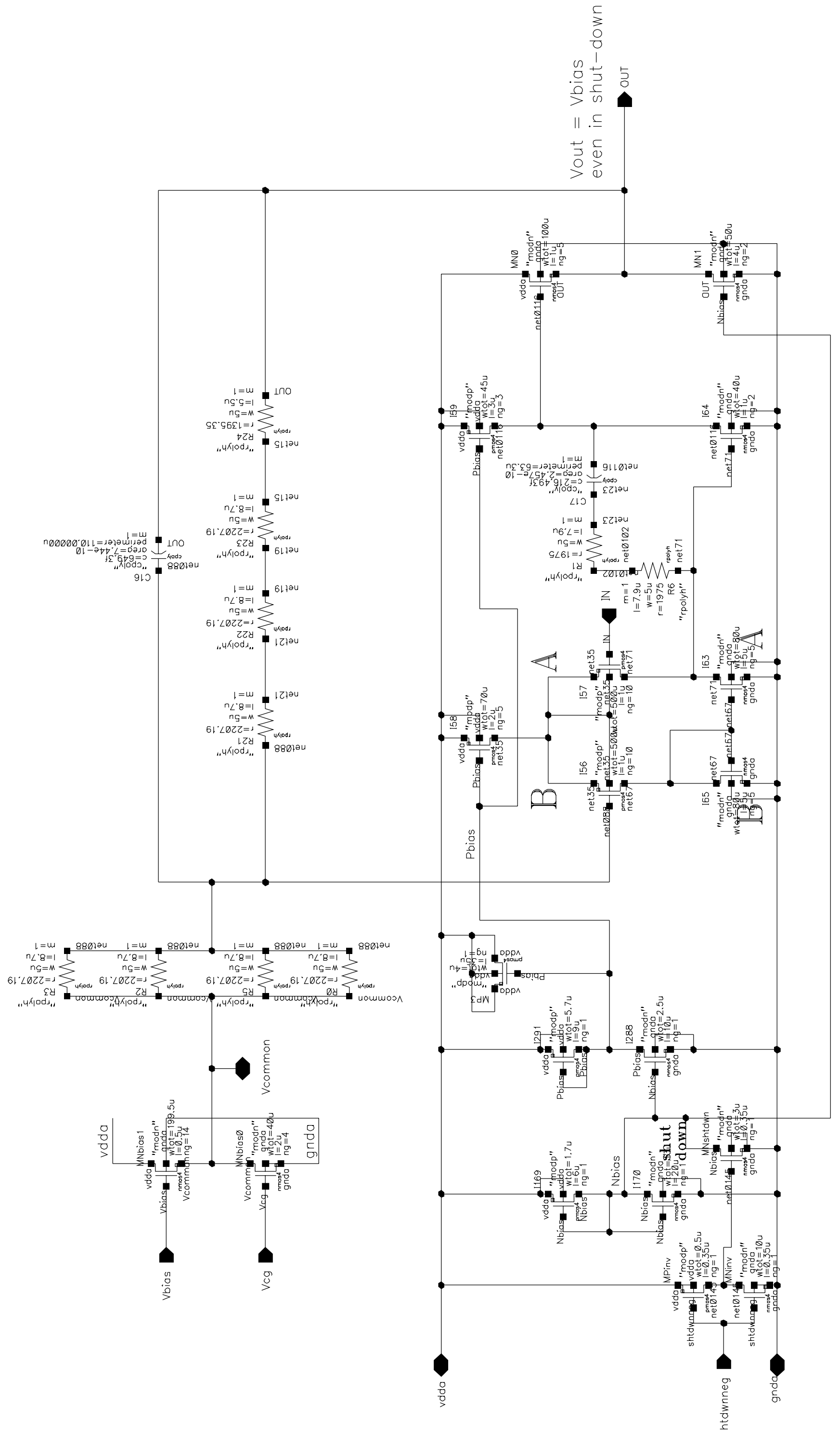


Figure 42: *n-XYTER* front-end schematic; cellname: FAST

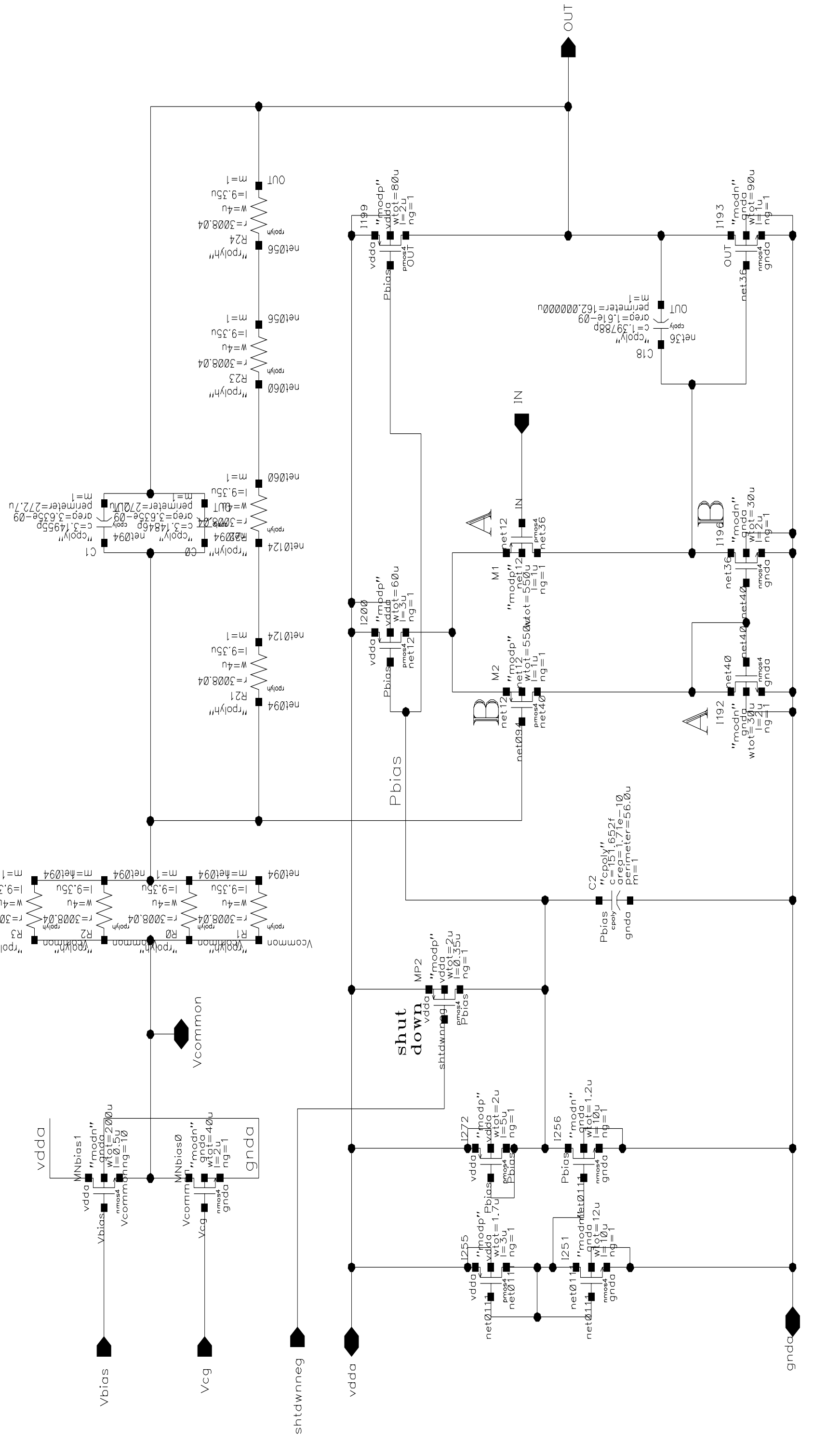


Figure 43: *n-XYTER* front-end schematic; cellname: SLOW1

B I/O Pads Description

A reference number has been assigned to each pad. The numbering starts in the upper left corner of the die (which is oriented with the analog input pads left) and runs counter-clockwise (cf. figure 44 for *n-XYTER 1.0*). The following tables summarize the signals and explain them. The pad coordinates refer to the center of the pad opening, which is 85 µm×85 µm, the exceptions for input pads and power supply ESD pads are annotated. Their enlarged pad windows are listed in section B.3. The origin of the coordinate system is defined by the lower left chip corner (0, 0). The dimensions of the chip die are 8 779.70 µm × 7 950.85 µm[1].

The analog input pads have a pitch of 101.4 µm, all others 100 µm

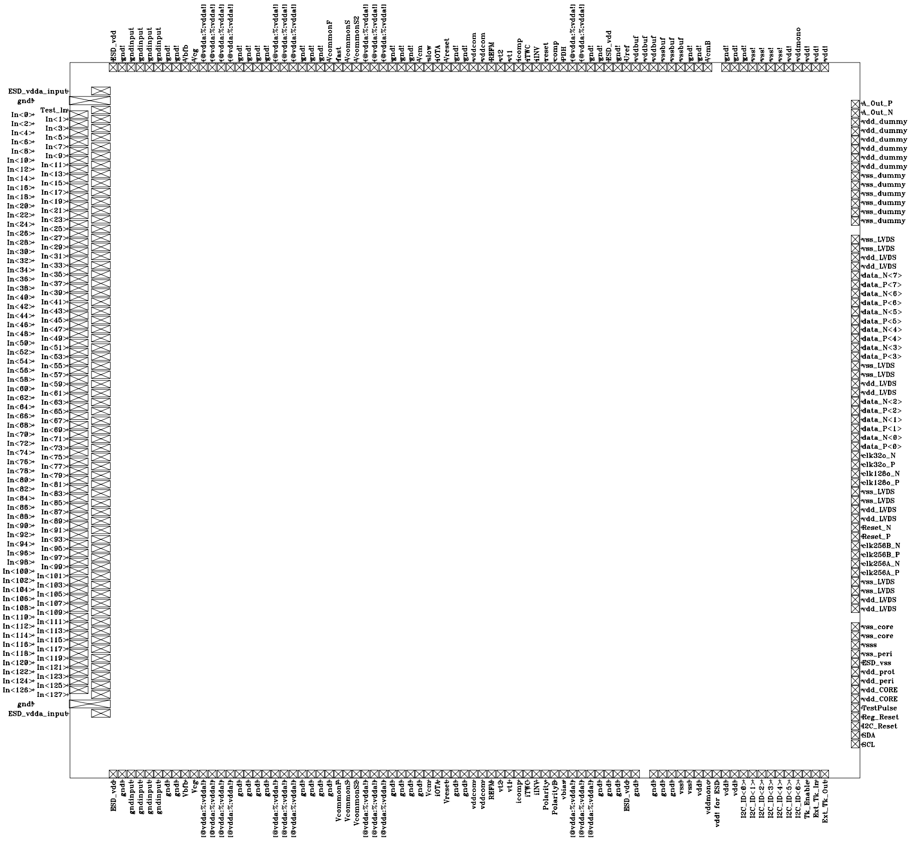


Figure 44: Pad layout of *n-XYTER 1.0*. The die size is $(8.8 \times 8.0)\,\mathrm{mm}^2$.

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[1] Note, that these are the dimensions of the chip's scribe line, i.e. not including cutting margins. They could add some 100 µm to the chip dimensions.

All PADS have 100 μm pitch, except the input PADS which have 101.4 μm.

The current magnitude is indicated very approximately for some pads as L (low, practically no DC current), or H (high, power supply current). All other pads are either I/O or monitor pads.

For I/O pads, direction is *output* by default. Input pads are identified by *input*.

Nominal values are intended as: DC level for a configuration for negative input charge (in parenthesis for positive input charge).

For current-bias monitor pads: positive current = current sunk by the chip.

Note for testing. The current generated by a DAC is normally sunk by a transistor in trans-diode configuration. A first test could be to read the voltage and to check whether it corresponds to the simulated value.

On the other hand, in order to really measure the current, the corresponding PAD must be kept at 3.3 V (for positive current; i.e. when a P-MOS is used in the circuit of the particular pad) or 0 V (for negative current; i.e. when a N-MOS is used). In this way, naturally, the internal circuitry will remain unbiased, so that the entire current sunk is indeed supplied through the pad and is thus measurable.

B.1 Front Pads

Num	Pin name	Type	Coordinates		Description	Suggested Connection	Values
			x [μm]	y [μm]			
1	`ESD_vdda_input`	analog power	352.50	7636.20	vdd bias for channel input pads ESD protection pad opening 205 μm × 85 μm	analog1 power	3.3 V *L*
2	`ESD_gnd!_input`	analog power	230.00	7529.80	gnd bias for channel input pads ESD protection pad opening 450 μm × 85 μm	analog1 ground	0.0 V *L*
3	`Test_In`	analog input	352.50	7426.90	Input of test channel pad opening 205 μm × 80 μm	external RC network output at pin	
4	`In<0>`	analog input	107.50	7376.20	Input of channel 0 pad opening 205 μm × 80 μm	input signal from the detector referred to analog ground	
5	`In<1>`	analog input	352.50	7325.50	Input of channel 1 pad opening 205 μm × 80 μm	input signal from the detector referred to analog ground	
6	`In<2>`	analog input	107.50	7274.80	Input of channel 2 pad opening 205 μm × 80 μm	input signal from the detector referred to analog ground	

Num	Pin name	Type	Coordinates		Description	Suggested Connection	Values
			x [µm]	y [µm]			
7	`In<3>`	analog input	352.50	7224.10	Input of channel 3 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
8	`In<4>`	analog input	107.50	7173.40	Input of channel 4 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
9	`In<5>`	analog input	352.50	7122.70	Input of channel 5 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
10	`In<6>`	analog input	107.50	7072.00	Input of channel 6 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
11	`In<7>`	analog input	352.50	7021.30	Input of channel 7 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
12	`In<8>`	analog input	107.50	6970.60	Input of channel 8 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
13	`In<9>`	analog input	352.50	6919.90	Input of channel 9 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
14	`In<10>`	analog input	107.50	6869.20	Input of channel 10 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
15	`In<11>`	analog input	352.50	6818.50	Input of channel 11 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
16	`In<12>`	analog input	107.50	6767.80	Input of channel 12 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	

Num	Pin name	Type	Coordinates x [µm]	 y [µm]	Description	Suggested Connection	Values
17	`In<13>`	analog input	352.50	6717.10	Input of channel 13 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
18	`In<14>`	analog input	107.50	6666.40	Input of channel 14 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
19	`In<15>`	analog input	352.50	6615.70	Input of channel 15 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
20	`In<16>`	analog input	107.50	6565.00	Input of channel 16 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
21	`In<17>`	analog input	352.50	6514.30	Input of channel 17 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
22	`In<18>`	analog input	107.50	6463.60	Input of channel 18 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
23	`In<19>`	analog input	352.50	6412.90	Input of channel 19 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
24	`In<20>`	analog input	107.50	6362.20	Input of channel 20 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
25	`In<21>`	analog input	352.50	6311.50	Input of channel 21 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
26	`In<22>`	analog input	107.50	6260.80	Input of channel 22 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	

Num	Pin name	Type	Coordinates		Description	Suggested Connection	Values
			x [µm]	y [µm]			
27	`In<23>`	analog input	352.50	6210.10	Input of channel 23 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
28	`In<24>`	analog input	107.50	6159.40	Input of channel 24 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
29	`In<25>`	analog input	352.50	6108.70	Input of channel 25 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
30	`In<26>`	analog input	107.50	6058.00	Input of channel 26 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
31	`In<27>`	analog input	352.50	6007.30	Input of channel 27 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
32	`In<28>`	analog input	107.50	5956.60	Input of channel 28 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
33	`In<29>`	analog input	352.50	5905.90	Input of channel 29 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
34	`In<30>`	analog input	107.50	5855.20	Input of channel 30 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
35	`In<31>`	analog input	352.50	5804.50	Input of channel 31 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
36	`In<32>`	analog input	107.50	5753.80	Input of channel 32 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	

Num	Pin name	Type	Coordinates x [µm]	 y [µm]	Description	Suggested Connection	Values
37	`In<33>`	analog input	352.50	5703.10	Input of channel 33 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
38	`In<34>`	analog input	107.50	5652.40	Input of channel 34 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
39	`In<35>`	analog input	352.50	5601.70	Input of channel 35 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
40	`In<36>`	analog input	107.50	5551.00	Input of channel 36 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
41	`In<37>`	analog input	352.50	5500.30	Input of channel 37 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
42	`In<38>`	analog input	107.50	5449.60	Input of channel 38 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
43	`In<39>`	analog input	352.50	5398.90	Input of channel 39 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
44	`In<40>`	analog input	107.50	5348.20	Input of channel 40 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
45	`In<41>`	analog input	352.50	5297.50	Input of channel 41 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
46	`In<42>`	analog input	107.50	5246.80	Input of channel 42 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	

Num	Pin name	Type	Coordinates x [µm]	 y [µm]	Description	Suggested Connection	Values
47	`In<43>`	analog input	352.50	5196.10	Input of channel 43 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
48	`In<44>`	analog input	107.50	5145.40	Input of channel 44 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
49	`In<45>`	analog input	352.50	5094.70	Input of channel 45 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
50	`In<46>`	analog input	107.50	5044.00	Input of channel 46 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
51	`In<47>`	analog input	352.50	4993.30	Input of channel 47 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
52	`In<48>`	analog input	107.50	4942.60	Input of channel 48 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
53	`In<49>`	analog input	352.50	4891.90	Input of channel 49 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
54	`In<50>`	analog input	107.50	4841.20	Input of channel 50 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
55	`In<51>`	analog input	352.50	4790.50	Input of channel 51 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
56	`In<52>`	analog input	107.50	4739.80	Input of channel 52 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	

Num	Pin name	Type	Coordinates x [µm]	 y [µm]	Description	Suggested Connection	Values
57	`In<53>`	analog input	352.50	4689.10	Input of channel 53 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
58	`In<54>`	analog input	107.50	4638.40	Input of channel 54 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
59	`In<55>`	analog input	352.50	4587.70	Input of channel 55 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
60	`In<56>`	analog input	107.50	4537.00	Input of channel 56 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
61	`In<57>`	analog input	352.50	4486.30	Input of channel 57 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
62	`In<58>`	analog input	107.50	4435.60	Input of channel 58 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
63	`In<59>`	analog input	352.50	4384.90	Input of channel 59 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
64	`In<60>`	analog input	107.50	4334.20	Input of channel 60 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
65	`In<61>`	analog input	352.50	4283.50	Input of channel 61 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
66	`In<62>`	analog input	107.50	4232.80	Input of channel 62 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	

Num	Pin name	Type	Coordinates x [µm]	Coordinates y [µm]	Description	Suggested Connection	Values
67	`In<63>`	analog input	352.50	4182.10	Input of channel 63 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
68	`In<64>`	analog input	107.50	4131.40	Input of channel 64 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
69	`In<65>`	analog input	352.50	4080.70	Input of channel 65 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
70	`In<66>`	analog input	107.50	4030.00	Input of channel 66 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
71	`In<67>`	analog input	352.50	3979.30	Input of channel 67 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
72	`In<68>`	analog input	107.50	3928.60	Input of channel 68 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
73	`In<69>`	analog input	352.50	3877.90	Input of channel 69 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
74	`In<70>`	analog input	107.50	3827.20	Input of channel 70 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
75	`In<71>`	analog input	352.50	3776.50	Input of channel 71 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
76	`In<72>`	analog input	107.50	3725.80	Input of channel 72 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	

Num	Pin name	Type	Coordinates x [µm]	 y [µm]	Description	Suggested Connection	Values
77	`In<73>`	analog input	352.50	3675.10	Input of channel 73 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
78	`In<74>`	analog input	107.50	3624.40	Input of channel 74 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
79	`In<75>`	analog input	352.50	3573.70	Input of channel 75 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
80	`In<76>`	analog input	107.50	3523.00	Input of channel 76 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
81	`In<77>`	analog input	352.50	3472.30	Input of channel 77 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
82	`In<78>`	analog input	107.50	3421.60	Input of channel 78 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
83	`In<79>`	analog input	352.50	3370.90	Input of channel 79 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
84	`In<80>`	analog input	107.50	3320.20	Input of channel 80 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
85	`In<81>`	analog input	352.50	3269.50	Input of channel 81 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
86	`In<82>`	analog input	107.50	3218.80	Input of channel 82 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	

Num	Pin name	Type	Coordinates x [µm]	 y [µm]	Description	Suggested Connection	Values
87	`In<83>`	analog input	352.50	3168.10	Input of channel 83 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
88	`In<84>`	analog input	107.50	3117.40	Input of channel 84 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
89	`In<85>`	analog input	352.50	3066.70	Input of channel 85 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
90	`In<86>`	analog input	107.50	3016.00	Input of channel 86 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
91	`In<87>`	analog input	352.50	2965.30	Input of channel 87 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
92	`In<88>`	analog input	107.50	2914.60	Input of channel 88 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
93	`In<89>`	analog input	352.50	2863.90	Input of channel 89 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
94	`In<90>`	analog input	107.50	2813.20	Input of channel 90 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
95	`In<91>`	analog input	352.50	2762.50	Input of channel 91 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
96	`In<92>`	analog input	107.50	2711.80	Input of channel 92 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	

Num	Pin name	Type	Coordinates x [µm]	 y [µm]	Description	Suggested Connection	Values
97	`In<93>`	analog input	352.50	2661.10	Input of channel 93 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
98	`In<94>`	analog input	107.50	2610.40	Input of channel 94 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
99	`In<95>`	analog input	352.50	2559.70	Input of channel 95 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
100	`In<96>`	analog input	107.50	2509.00	Input of channel 96 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
101	`In<97>`	analog input	352.50	2458.30	Input of channel 97 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
102	`In<98>`	analog input	107.50	2407.60	Input of channel 98 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
103	`In<99>`	analog input	352.50	2356.90	Input of channel 99 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
104	`In<100>`	analog input	107.50	2306.20	Input of channel 100 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
105	`In<101>`	analog input	352.50	2255.50	Input of channel 101 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
106	`In<102>`	analog input	107.50	2204.80	Input of channel 102 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	

Num	Pin name	Type	Coordinates x [µm]	 y [µm]	Description	Suggested Connection	Values
107	`In<103>`	analog input	352.50	2154.10	Input of channel 103 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
108	`In<104>`	analog input	107.50	2103.40	Input of channel 104 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
109	`In<105>`	analog input	352.50	2052.70	Input of channel 105 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
110	`In<106>`	analog input	107.50	2002.00	Input of channel 106 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
111	`In<107>`	analog input	352.50	1951.30	Input of channel 107 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
112	`In<108>`	analog input	107.50	1900.60	Input of channel 108 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
113	`In<109>`	analog input	352.50	1849.90	Input of channel 109 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
114	`In<110>`	analog input	107.50	1799.20	Input of channel 110 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
115	`In<111>`	analog input	352.50	1748.50	Input of channel 111 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
116	`In<112>`	analog input	107.50	1697.80	Input of channel 112 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	

Num	Pin name	Type	Coordinates x [µm]	 y [µm]	Description	Suggested Connection	Values
117	`In<113>`	analog input	352.50	1647.10	Input of channel 113 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
118	`In<114>`	analog input	107.50	1596.40	Input of channel 114 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
119	`In<115>`	analog input	352.50	1545.70	Input of channel 115 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
120	`In<116>`	analog input	107.50	1495.00	Input of channel 116 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
121	`In<117>`	analog input	352.50	1444.30	Input of channel 117 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
122	`In<118>`	analog input	107.50	1393.60	Input of channel 118 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
123	`In<119>`	analog input	352.50	1342.90	Input of channel 119 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
124	`In<120>`	analog input	107.50	1292.20	Input of channel 120 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
125	`In<121>`	analog input	352.50	1241.50	Input of channel 121 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
126	`In<122>`	analog input	107.50	1190.80	Input of channel 122 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	

Num	Pin name	Type	Coordinates x [µm]	y [µm]	Description	Suggested Connection	Values
127	`In<123>`	analog input	352.50	1140.10	Input of channel 123 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
128	`In<124>`	analog input	107.50	1089.40	Input of channel 124 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
129	`In<125>`	analog input	352.50	1038.70	Input of channel 125 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
130	`In<126>`	analog input	107.50	988.00	Input of channel 126 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
131	`In<127>`	analog input	352.50	937.30	Input of channel 127 pad opening 205 µm × 80 µm	input signal from the detector referred to analog ground	
132	`ESD_gnda_input`	analog power	230.00	833.40	gnd bias for channel input pads ESD protection pad opening 450 µm × 85 µm	analog1 ground	0.0 V *L*
133	`ESD_vdda_input`	analog power	352.50	727.00	vdd bias for channel input pads ESD protection pad opening 205 µm × 85 µm	analog1 power	3.3 V *L*

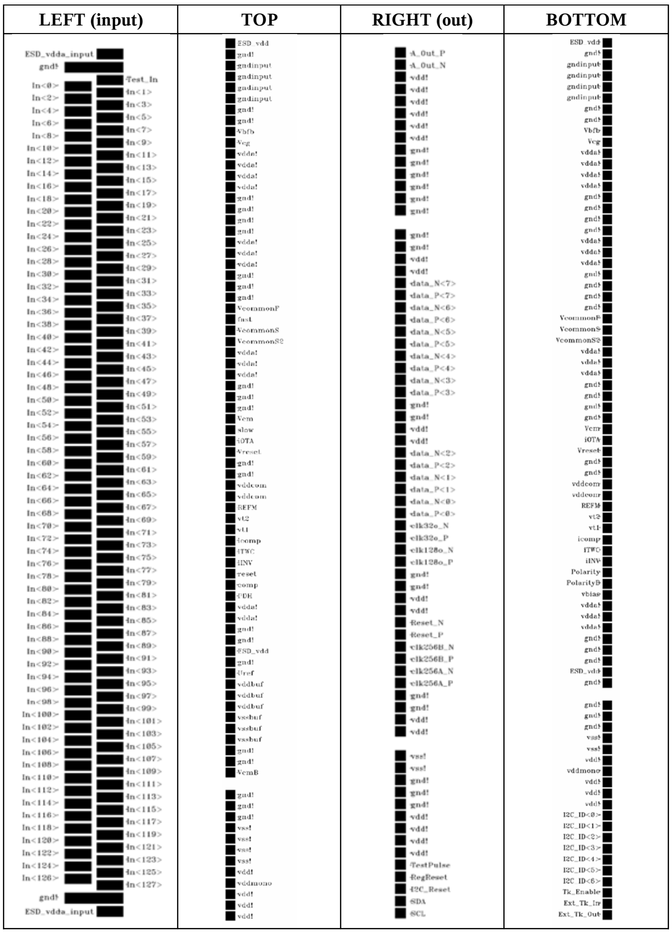

Figure 45: LEFT (input), TOP, RIGHT (out), BOTTOM

B.2 Bottom Pads

Num	Pin name	Type	Coordinates x [µm]	 y [µm]	Description	Suggested Connection	Values
134	`ESD_vdda`	analog power	489.30	52.90	vdd bias for analog pads ESD protection	analog1 power	3.3 V *L*
135	`ESD_gnda!`	analog power	589.30	52.90	gnd bias for analog pads ESD protection	analog1 ground	0 V *L*
136	`gndinput`	analog power	689.30	52.90	signal ground for the input transistor	analog1 ground	0 V *H*
137	`gndinput`	analog power	789.30	52.90	signal ground for the input transistor	analog1 ground	0 V *H*
138	`gndinput`	analog power	889.30	52.90	signal ground for the input transistor	analog1 ground	0 V *H*
139	`gndinput`	analog power	989.30	52.90	signal ground for the input transistor	analog1 ground	0 V *H*
140	`gnd!`	analog power	1089.30	52.90	analog ground	analog1 ground	0 V *H*
141	`gnd!`	analog power	1189.30	52.90	analog ground	analog1 ground	0 V *H*
142	`Vbfb`	analog output	1289.30	52.90	bypass/monitor pad for Vbfb (bias for preamplifier feedback transistor); DAC register number 19	optional diagnostic test pad with 100 nF capacitor	1.2 V for negative input charge; (1.4 V for positive input charge)
143	`Vcg`	analog output	1389.30	52.90	bypass/monitor pad for Vcg (bias for preamplifier current); DAC register number 16	optional diagnostic test pad with 100 nF capacitor	1.398 V 187 µA
144	`vdda!`	analog power	1489.30	52.90	analog power	analog1 power	3.3 V *H*
145	`vdda!`	analog power	1589.30	52.90	analog power	analog1 power	3.3 V *H*
146	`vdda!`	analog power	1689.30	52.90	analog power	analog1 power	3.3 V *H*
147	`vdda!`	analog power	1789.30	52.90	analog power	analog1 power	3.3 V *H*
148	`gnd!`	analog power	1889.30	52.90	analog ground	analog1 ground	0 V *H*
149	`gnd!`	analog power	1989.30	52.90	analog ground	analog1 ground	0 V *H*
150	`gnd!`	analog power	2089.30	52.90	analog ground	analog1 ground	0 V *H*
151	`gnd!`	analog power	2189.30	52.90	analog ground	analog1 ground	0 V *H*

Num	Pin name	Type	Coordinates x [µm]	 y [µm]	Description	Suggested Connection	Values
152	`vdda!`	analog power	2289.30	52.90	analog power	analog1 power	3.3 V *H*
153	`vdda!`	analog power	2389.30	52.90	analog power	analog1 power	3.3 V *H*
154	`vdda!`	analog power	2489.30	52.90	analog power	analog1 power	3.3 V *H*
155	`gnd!`	analog power	2589.30	52.90	analog ground	analog1 ground	0 V *H*
156	`gnd!`	analog power	2689.30	52.90	analog ground	analog1 ground	0 V *H*
157	`gnd!`	analog power	2789.30	52.90	analog ground	analog1 ground	0 V *H*
158	`gnd!`	analog power	2889.30	52.90	analog ground	analog1 ground	0 V *H*
159	`VcommonF`	analog output	2989.30	52.90	bypass/monitor pad for VcommonF (bias voltage for Fast shaper) related to DAC rgister number=20	optional diagnostic test pad with 100 nF capacitor	0.563 V for negative input charge; (0.513 V for postive input charge)
160	`VcommonS`	analog output	3089.30	52.90	bypass/monitor pad for VcommonS (bias voltage for slow shaper – stage 1) related to DAC register number = 22	optional diagnostic test pad with 100 nF capacitor	0.564 V negative input charge (0.558 V positive input charge)
161	`VcommonS2`	analog output	3189.30	52.90	bypass/monitor pad for VcommonS2 (bias voltage for Slow shaper – stage 2) related to DAC register number = 22	optional diagnostic test pad with 100 nF capacitor	0.465 V negative input charge (0.537 V positive input charge)
162	`vdda!`	analog power	3289.30	52.90	analog power	analog1 power	3.3 V *H*
163	`vdda!`	analog power	3389.30	52.90	analog power	analog1 power	3.3 V *H*

Num	Pin name	Type	Coordinates		Description	Suggested Connection	Values
			x [µm]	y [µm]			
164	`vdda!`	analog power	3489.30	52.90	analog power	analog1 power	3.3 V *H*
165	`gnda`	analog power	3589.30	52.90	analog ground	analog1 ground	0.0 V *H*
166	`gnda`	analog power	3689.30	52.90	analog ground	analog1 ground	0.0 V *H*
167	`gnda`	analog power	3789.30	52.90	analog ground	analog1 ground	0.0 V *H*
168	`gnda`	analog power	3889.30	52.90	analog ground	analog1 ground	0.0 V *H*
169	`Vcm`	analog output	3989.30	52.90	bias voltage for the slow shaper and analog memory	optional diagnostic test pad with 100 nF capacitor	
170	`iOTA`	analog output	4089.30	52.90	bypass/monitor pad for iOTA (iPDH)(bias current for PDH) DAC Register number = 28	optional diagnostic test pad	0.8 V - 80 µA
171	`Vreset`	analog power	4189.30	52.90	reset voltage level for PDH (nominally it has to be tied to gnd)	analog ground	0 V (gnd) *H*
172	`gndcmp`	analog power	4289.30	52.90	gnd comparator (bulk)	analog2 ground	0 V (gnd) *H*
173	`gndcmp`	analog power	4389.30	52.90	gnd comparator (bulk)	analog2 ground	0 V (gnd) *H*
174	`vddcmp`	analog power	4489.30	52.90	comparator vdd	analog2 power	3.3 V *H*
175	`vddcmp`	analog power	4589.30	52.90	comparator vdd	analog2 power	3.3 V *H*
176	`REFM`	analog output	4689.30	52.90	bypass/monitor for DACs reference voltage (from band-gap ref.)	optional diagnostic test pad with 100 nF capacitor	1.382 V
177	`vt2`	analog output	4789.30	52.90	bypass/monitor pad for vt2 (threshold voltage 2) DAC register number = 18 and 33bit2 (polarity)	optional diagnostic test pad with 100 nF capacitor	vdd-40 mV ? negative input charge (vdd) V positive input charge

Num	Pin name	Type	Coordinates x [µm]	 y [µm]	Description	Suggested Connection	Values
178	`vt1`	analog output	4889.30	52.90	bypass/monitor pad for vt1 (threshold voltage 1) DAC register number = 18 and 33bit2 (polarity)	optional diagnostic test pad with 100 nF capacitor	vdd negative input charge (vdd-40 mV?) positive input charge
179	`icomp`	analog output	4989.30	52.90	bypass/monitor pad for iCOMP (bias current for comparator) DAC register number=25	optional diagnostic test pad	0.68 V -50 µA
180	`iTWC`	analog output	5089.30	52.90	bypass/monitor pad for iTWC (bias current for the TWC) DAC register number = 29	test pad	0.929 V -60 µA
181	`iINV`	analog output	5189.30	52.90	bypass/monitor pad for iINV (bias current for the comparator output-inverter) DAC register number = 27	optional diagnostic test pad	1.8 V 37 µA
182	`Polarity`	analog input	5289.30	52.90	monitor pad for input charge polarity selector (active high) - overrides internal setting	optional external logic network to select the polarity of the pulse	Z
183	`PolarityB`	analog input	5389.30	52.90	monitor pad for input charge polarity selector NEG - overrides internal setting	optional external logic network to select the polarity of the pulse	Z
184	`vbias`	analog output	5489.30	52.90	bypass/monitor pad for vbias (bias for analogue memory OPA) internally generated from REFM	optional diagnostic test pad with 100 nF capacitor	2.4 V
185	`vdda!`	analog power	5589.30	52.90	analog power	analog1 power	3.3 V *H*
186	`vdda!`	analog power	5689.30	52.90	analog power	analog1 power	3.3 V *H*
187	`vdda!`	analog power	5789.30	52.90	analog power	analog1 power	3.3 V *H*

Num	Pin name	Type	Coordinates		Description	Suggested Connection	Values
			x [µm]	y [µm]			
188	`gnda`	analog power	5889.30	52.90	analog ground	analog1 ground	0 V *H*
189	`gnda`	analog power	5989.30	52.90	analog ground	analog1 ground	0 V *H*
190	`gnda`	analog power	6089.30	52.90	analog ground	analog1 ground	0 V *H*
191	`ESD_vdda`	analog power	6189.30	52.90	vdd bias for analog pads ESD protection	analog1 power	3.3 V *L*
192	`ESD_gnda!`	analog power	6289.30	52.90	gnd bias for analog pads ESD protection	analog1 ground	0 V *H*
193	`gnd!`	digital power	6489.30	52.90	digital ground - substrate	digital ground	0 V *H*
194	`gnd!`	digital power	6589.30	52.90	digital ground - substrate	digital ground	0 V *H*
195	`gnd!`	digital power	6689.30	52.90	digital ground - substrate	digital ground	0 V *H*
196	`vss!`	digital power	6789.30	52.90	digital ground	digital ground	0 V *H*
197	`vss!`	digital power	6889.30	52.90	digital ground	digital ground	0 V *H*
198	`vdd!`	digital power	6989.30	52.90	digital power	digital power	3.3 V *H*
199	`vddmono`	digital power	7089.30	52.90	vdd monostable	analog3 power	3.3 V *H*
200	`vdd!`	digital power	7189.30	52.90	digital power	digital power	3.3 V *H*
201	`vdd!`	digital power	7289.30	52.90	digital power	digital power	3.3 V *H*
202	`vdd!`	digital power	7389.30	52.90	digital power	digital power	3.3 V *H*
203	`I2C_ID<0>`	digital input pull-down trigger	7489.30	52.90	bit0 of chip address	connect an external logic network to change the chip address	0-3.3 V input
204	`I2C_ID<1>`	digital input pull-down trigger	7589.30	52.90	bit1 of chip address	connect an external logic network to change the chip address	0-3.3 V input
205	`I2C_ID<2>`	digital input pull-down trigger	7689.30	52.90	bit2 of chip address	connect an external logic network to change the chip address	0-3.3 V input
206	`I2C_ID<3>`	digital input pull-down trigger	7789.30	52.90	bit3 of chip address	connect an external logic network to change the chip address	0-3.3 V input

Num	Pin name	Type	Coordinates x [µm]	y [µm]	Description	Suggested Connection	Values
207	`I2C_ID<4>`	digital input pull-down trigger	7889.30	52.90	bit4 of chip address	connect an external logic network to change the chip address	0-3.3 V input
208	`I2C_ID<5>`	digital input pull-down trigger	7989.30	52.90	bit5 of chip address	connect an external logic network to change the chip address	0-3.3 V input
209	`I2C_ID<6>`	digital input pull-down trigger	8089.30	52.90	bit6 of chip address	connect an external logic network to change the chip address	0-3.3 V input
210	`Tk_Enable`	digital input pullup trigger	8189.30	52.90	token manager enable - iternally pulled up	if connected to ground the external token manager connected between `Ext_Tk_In`, `Ext_Tk_Out` should inject the token. This pin should be pulled up for normal operation	3.3V input
211	`Ext_Tk_In`	digital input pull-down trigger	8289.30	52.90	external input token, with pull-down (used only when `Tk_Enable=0`)	if `Tk_Enable` = 0 an external token manager provides the readout token	0-3.3 V input
212	`Ext_Tk_Out`	digital output	8389.30	52.90	external output token (a token will be output only if if `Tk_Enable` = 0	0-3.3 V input	

B.3 Backside Pads

Num	Pin name	Type	Coordinates x [µm]	 y [µm]	Description	Suggested Connection	Values
213	`SCL`	digital input pullup trigger	8726.80	390.35	clock for the I^{2}C	clock to operate the I^{2}C	
214	`SDA`	digital bidirectional	8726.80	490.35	I^{2}C data (bidirectional)	bidirectional pin	
215	`I2C_Reset`	digital input pullup trigger	8726.80	590.35	reset of the I^{2}C interface logic (active low)		
216	`RegReset`	digital input pullup trigger	8726.80	690.35	resets I^{2}C registers to default (active low)		
217	`TestPulse`	digital input pulldown trigger	8726.80	790.35	test pulse trigger (active low) - internally pulled down		
218	`vddcore`	digital power	8726.80	890.35	digital power	digital power	
219	`vddcore`	digital power	8726.80	990.35	digital power	digital power	
220	`vdd!`	digital power	8726.80	1090.35	digital power	digital power	
221	`vdd!`	digital power	8726.80	1190.35	digital power	digital power	
222	`gnd!`	digital power	8726.80	1290.35	digital ground	digital ground	
223	`gnd!`	digital power	8726.80	1390.35	digital ground	digital ground	
224	`gnd!`	digital power	8726.80	1490.35	digital ground	digital ground	
225	`vss!`	digital power	8726.80	1590.35	digital ground	digital ground	
226	`vss!`	digital power	8726.80	1690.35	digital ground	digital ground	
227	`vdd!`	digital power	8726.80	1890.35	digital power	digital power	
228	`vdd!`	digital power	8726.80	1990.35	digital power	digital power	
229	`gnd!`	digital power	8726.80	2090.35	digital ground	digital ground	
230	`gnd!`	digital power	8726.80	2190.35	digital ground	digital ground	
231	`clk256A_P`	LVDSI	8726.80	2290.35	primary clock input	LVDS clock signal	
232	`clk256A_N`	LVDSI	8726.80	2390.35	primary clock input	LVDS clock signal	

Num	Pin name	Type	Coordinates		Description	Suggested Connection	Values
			x [µm]	y [µm]			
233	`clk256B_P`	LVDSI	8726.80	2490.35	secondary clock input	LVDS clock signal	
234	`clk256B_N`	LVDSI	8726.80	2590.35	secondary clock input	LVDS clock signal	
235	`Reset_P`	LVDSI	8726.80	2690.35	synchronous reset of the time-stamp generator	LVDS reset signal	
236	`Reset_N`	LVDSI	8726.80	2790.35	synchronous reset of the time-stamp generator	LVDS reset signal	
237	`vdd!`	digital power	8726.80	2890.35	digital power	digital power	
238	`vdd!`	digital power	8726.80	2990.35	digital power	digital power	
239	`gnd!`	digital power	8726.80	3090.35	digital ground	digital ground	
240	`gnd!`	digital power	8726.80	3190.35	digital ground	digital ground	
241	`clk128o_P`	LVDS output	8726.80	3290.35	clock divider output		
242	`clk128o_N`	LVDS output	8726.80	3390.35	clock divider output		
243	`clk32o_P`	LVDS output	8726.80	3490.35	clock divider output	clock to operate external ADC	
244	`clk32o_N`	LVDS output	8726.80	3590.35	clock divider output	clock to operate external ADC	
245	`data_P<0>`	LVDS output	8726.80	3690.35	output data bus		
246	`data_N<0>`	LVDS output	8726.80	3790.35	output data bus		
247	`data_P<1>`	LVDS output	8726.80	3890.35	output data bus		
248	`data_N<1>`	LVDS output	8726.80	3990.35	output data bus		
249	`data_P<2>`	LVDS output	8726.80	4090.35	output data bus		
250	`data_N<2>`	LVDS output	8726.80	4190.35	output data bus		
251	`vdd!`	digital power	8726.80	4290.35	digital power	digital power	
252	`vdd!`	digital power	8726.80	4390.35	digital power	digital power	
253	`gnd!`	digital power	8726.80	4490.35	digital ground	digital ground	
254	`gnd!`	digital power	8726.80	4590.35	digital ground	digital ground	
255	`data_P<3>`	LVDS output	8726.80	4690.35	output data bus		

Num	Pin name	Type	Coordinates x [µm]	Coordinates y [µm]	Description	Suggested Connection	Values
256	`data_N<3>`	LVDS output	8726.80	4790.35	output data bus		
257	`data_P<4>`	LVDS output	8726.80	4890.35	output data bus		
258	`data_N<4>`	LVDS output	8726.80	4990.35	output data bus		
259	`data_P<5>`	LVDS output	8726.80	5090.35	output data bus		
260	`data_N<5>`	LVDS output	8726.80	5190.35	output data bus		
261	`data_P<6>`	LVDS output	8726.80	5290.35	output data bus		
262	`data_N<6>`	LVDS output	8726.80	5390.35	output data bus		
263	`data_P<7>`	LVDS output	8726.80	5490.35	output data bus		
264	`data_N<7>`	LVDS output	8726.80	5590.35	output data bus		
265	**`vdd!`**	digital power	8726.80	5690.35	digital power	digital power	
266	**`vdd!`**	digital power	8726.80	5790.35	digital power	digital power	
267	**`gnd!`**	digital power	8726.80	5890.35	digital ground	digital ground	
268	**`gnd!`**	digital power	8726.80	5990.35	digital ground	digital ground	
269	**`gnd!`**	digital power	8726.80	6190.35	digital ground	digital ground	
270	**`gnd!`**	digital power	8726.80	6290.35	digital ground	digital ground	
271	**`gnd!`**	digital power	8726.80	6390.35	digital ground	digital ground	
272	**`gnd!`**	digital power	8726.80	6490.35	digital ground	digital ground	
273	**`gnd!`**	digital power	8726.80	6590.35	digital ground	digital ground	
274	**`gnd!`**	digital power	8726.80	6690.35	digital ground	digital ground	
275	**`vdd!`**	digital power	8726.80	6790.35	digital power	digital power	
276	**`vdd!`**	digital power	8726.80	6890.35	digital power	digital power	
277	**`vdd!`**	digital power	8726.80	6990.35	digital power	digital power	
278	**`vdd!`**	digital power	8726.80	7090.35	digital power	digital power	
279	**`vdd!`**	digital power	8726.80	7190.35	digital power	digital power	
280	**`vdd!`**	digital power	8726.80	7290.35	digital power	digital power	

Num	Pin name	Type	Coordinates x [µm]	 y [µm]	Description	Suggested Connection	Values
281	`A_Out_N`	analog output differential	8726.80	7390.35	analog output for amplitude measurements	external ADC or measurement device	
282	`A_Out_P`	analog output differential	8726.80	7490.35	analog output for amplitude measurements	external ADC or measurement device	

B.4 Top Pads

Num	Pin name	Type	Coordinates		Description	Suggested Connection	Values
			x [µm]	y [µm]			
283	`vdd!`	digital power	8389.30	7897.95	digital power	digital power	
284	`vdd!`	digital power	8289.30	7897.95	digital power	digital power	
285	`vdd!`	digital power	8189.30	7897.95	digital power	digital power	
286	`vddmono`	digital power	8089.30	7897.95	vdd monostable	analog3 power	
287	`vdd!`	digital power	7989.30	7897.95	digital power	digital power	
288	`vss!`	digital power	7889.30	7897.95	digital ground	digital ground	
289	`vss!`	digital power	7789.30	7897.95	digital ground	digital ground	
290	`vss!`	digital power	7689.30	7897.95	digital ground	digital ground	
291	`vss!`	digital power	7589.30	7897.95	digital ground	digital ground	
292	`gnd!`	digital power	7489.30	7897.95	digital ground	digital ground	
293	`gnd!`	digital power	7389.30	7897.95	digital ground	digital ground	
294	`gnd!`	digital power	7289.30	7897.95	digital ground	digital ground	
295	`VcmB`	analog output	7089.30	7897.95	output buffer common mode voltage	optional diagnostic test pad with 100 nF capacitor	
296	`gndbuf`	analog power	6989.30	7897.95	analog ground	analog4 ground	
297	`gndbuf`	analog power	6889.30	7897.95	analog ground	analog4 ground	
298	`vssbuf`	analog power	6789.30	7897.95	analog ground	analog4 ground	
299	`vssbuf`	analog power	6689.30	7897.95	analog ground	analog4 ground	
300	`vssbuf`	analog power	6589.30	7897.95	analog ground	analog4 ground	
301	`vddbuf`	analog power	6489.30	7897.95	analog power	analog4 power	
302	`vddbuf`	analog power	6389.30	7897.95	analog power	analog4 power	
303	`vddbuf`	analog power	6289.30	7897.95	analog power	analog4 power	

Num	Pin name	Type	Coordinates x [µm]	 y [µm]	Description	Suggested Connection	Values
304	`Uref`	analog output	6189.30	7897.95	reference voltage of the output buffer	optional diagnostic test pad with 100 nF capacitor	
305	`ESD_gnda`	analog power	6089.30	7897.95	gnd bias for analog pads EDS protection	gnd bias for analog pads EDS protection	
306	`ESD_vdda`	analog power	5989.30	7897.95	vdd bias for analog pads ESD protection	analog1 power	
307	`gnda`	analog power	5889.30	7897.95	analog ground	analog1 ground	
308	`gnda`	analog power	5789.30	7897.95	analog ground	analog1 ground	
309	`vdda!`	analog power	5689.30	7897.95	analog power	analog1 power	
310	`vdda!`	analog power	5589.30	7897.95	analog power	analog1 power	
311	`PDH`	analog output	5489.30	7897.95	test channel peak detector and hold	optional diagnostic test pad	
312	`comp`	analog output	5389.30	7897.95	comparator output of the test channel	optional diagnostic test pad	
313	`reset`	analog output	5289.30	7897.95	test channel reset level voltage	optional diagnostic test pad	
314	`iINV`	analog output	5189.30	7897.95	bias current for the comparator	optional diagnostic test pad	
315	`iTWC`	analog output	5089.30	7897.95	bias current for the time walk compensation	optional diagnostic test pad	
316	`icomp`	analog output	4989.30	7897.95	bias current for the comparator	optional diagnostic test pad	
317	`vt1`	analog output	4889.30	7897.95	threshold voltage 1	optional diagnostic test pad with 100 nF capacitor	
318	`vt2`	analog output	4789.30	7897.95	threshold voltage 2	optional diagnostic test pad with 100 nF capacitor	

Num	Pin name	Type	Coordinates x [µm]	y [µm]	Description	Suggested Connection	Values
319	`REFM`	analog output	4689.30	7897.95	internal bandgap voltage reference	optional diagnostic test pad with 100 nF capacitor	
320	`vddcomp`	analog power	4589.30	7897.95	vdd comparator	analog2 power	
321	`vddcomp`	analog power	4489.30	7897.95	vdd comparator	analog2 power	
322	`vsscomp`	analog power	4389.30	7897.95	analog ground	analog2 ground	
323	`vsscomp`	analog power	4289.30	7897.95	analog ground	analog2 ground	
324	`Vreset`	analog output	4189.30	7897.95	reset voltage level for the peak detector	analog ground	
325	`iOTA`	analog output	4089.30	7897.95	bias current for the peak detector and hold	optional diagnostic test pad	
326	`slow`	analog output	3989.30	7897.95	channel slow shaper output	optional diagnostic test pad	
327	`Vcm`	analog output	3889.30	7897.95	bias voltage for the slow shaper and analog memory	optional diagnostic test pad with 100 nF capacitor	
328	`gnda`	analog power	3789.30	7897.95	analog ground	analog1 ground	
329	`gnda`	analog power	3689.30	7897.95	analog ground	analog1 ground	
330	`gnda`	analog power	3589.30	7897.95	analog ground	analog1 ground	
331	`vdda!`	analog power	3489.30	7897.95	analog power	analog1 power	
332	`vdda!`	analog power	3389.30	7897.95	analog power	analog1 power	
333	`vdda!`	analog power	3289.30	7897.95	analog power	analog1 power	
334	`VcommonS2`	analog output	3189.30	7897.95	bias voltage for slow shaper stage2	optional diagnostic test pad with 100 nF capacitor	
335	`VcommonS`	analog output	3089.30	7897.95	bias voltage for slow shaper stage1	optional diagnostic test pad with 100 nF capacitor	
336	`fast`	analog output	2989.30	7897.95	fast shaper output of the test channel	optional diagnostic test pad	

Num	Pin name	Type	Coordinates x [µm]	 y [µm]	Description	Suggested Connection	Values
337	`VcommonF`	analog output	2889.30	7897.95	bias voltage for fast shaper	optional diagnostic test pad with 100 nF capacitor	
338	`gnd!`	analog power	2789.30	7897.95	analog ground	analog1 ground	
339	`gnd!`	analog power	2689.30	7897.95	analog ground	analog1 ground	
340	`gnd!`	analog power	2589.30	7897.95	analog ground	analog1 ground	
341	`vdda!`	analog power	2489.30	7897.95	analog power	analog1 power	
342	`vdda!`	analog power	2389.30	7897.95	analog power	analog1 power	
343	`vdda!`	analog power	2289.30	7897.95	analog power	analog1 power	
344	`gnd!`	analog power	2189.30	7897.95	analog ground	analog1 ground	
345	`gnd!`	analog power	2089.30	7897.95	analog ground	analog1 ground	
346	`gnd!`	analog power	1989.30	7897.95	analog ground	analog1 ground	
347	`gnd!`	analog power	1889.30	7897.95	analog ground	analog1 ground	
348	`vdda!`	analog power	1789.30	7897.95	analog power	analog1 power	
349	`vdda!`	analog power	1689.30	7897.95	analog power	analog1 power	
350	`vdda!`	analog power	1589.30	7897.95	analog power	analog1 power	
351	`vdda!`	analog power	1489.30	7897.95	analog power	analog1 power	
352	`Vcg`	analog power	1389.30	7897.95	bias for preamplifier feedback transistor	optional diagnostic test pad with 100 nF capacitor	
353	`Vbfb`	analog power	1289.30	7897.95	bias for preamplifier feedback transistor	optional diagnostic test pad with 100 nF capacitor	
354	`gnda`	analog power	1189.30	7897.95	analog ground	analog1 ground	
355	`gnda`	analog power	1089.30	7897.95	analog ground	analog1 ground	
356	`gndinput`	analog power	989.30	7897.95	signal ground for the input transistor	analog1 ground	
357	`gndinput`	analog power	889.30	7897.95	signal ground for the input transistor	analog1 ground6	

Num	Pin name	Type	Coordinates x [µm]	Coordinates y [µm]	Description	Suggested Connection	Values
358	`gndinput`	analog power	789.30	7897.95	signal ground for the input transistor	analog1 ground	
359	`gndinput`	analog power	689.30	7897.95	signal ground for the input transistor	analog1 ground	
360	`ESD_gnd_analog`	analog power	589.30	7897.95	gnd bias for analog pads EDS protection	gnd bias for analog pads EDS protection	
361	`ESD_vdd_analog`	analog power	489.30	7897.95	vdd bias for analog pads ESD protection	analog1 power	

C Input Impedance Simulations

This chapter presents simulations on the dynamic input impedance of the front-end. Figure 46 shows the schematic underlying these simulations. The input capacitance was split into two capacitances, C_c simulates the inter-channel capacitance. Here Z_{in} is calculated excluding C_c.

In this way the coupling is then calculated by:

$$\frac{Z_{in}}{(Z_{in} + Z_c)} \qquad \text{where} \qquad Z_c = \frac{1}{j\omega C_c}$$

Simulations were performed taking $C_c = 0.3C_{tot}$ and $C_c = 0.9C_{tot}$ whrere $C_{tot} = 30\ pF$.

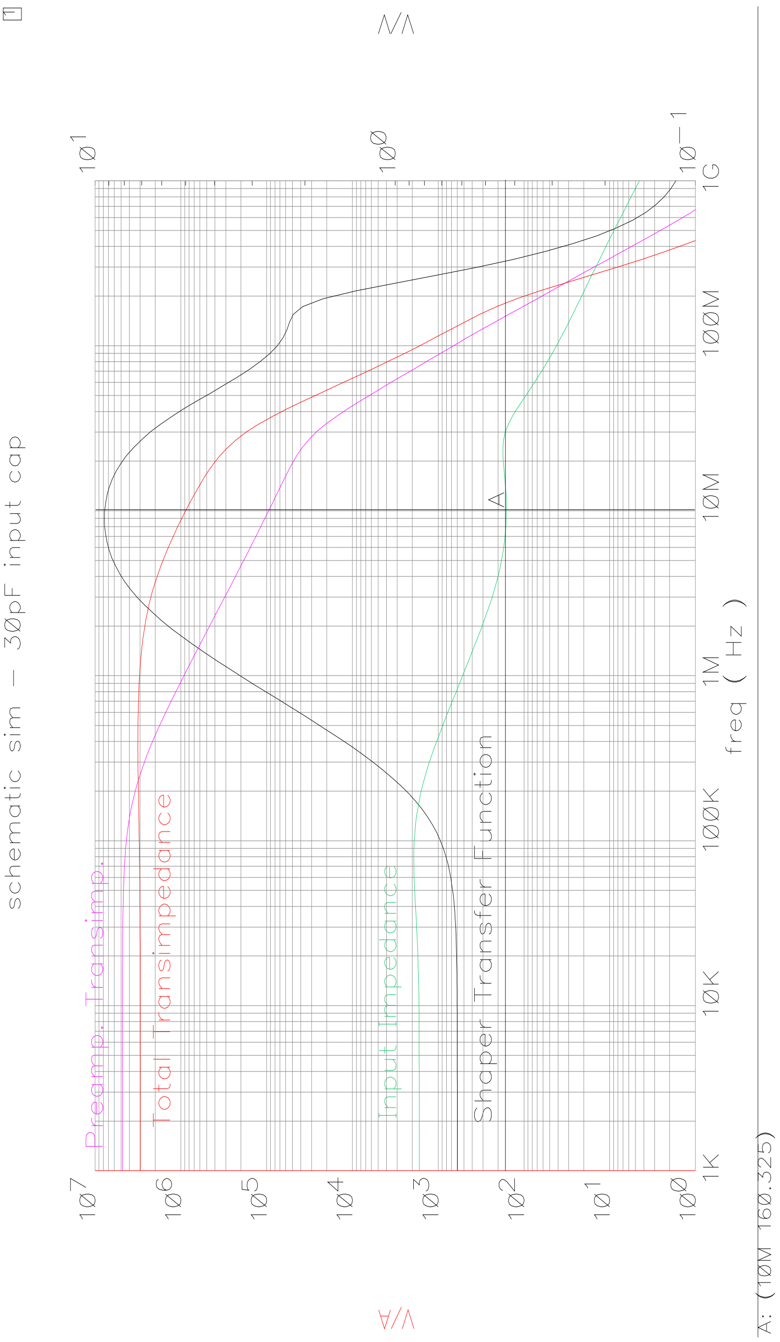

Figure 47: Input Impedence vs. frequency, with interchannel coupling effects

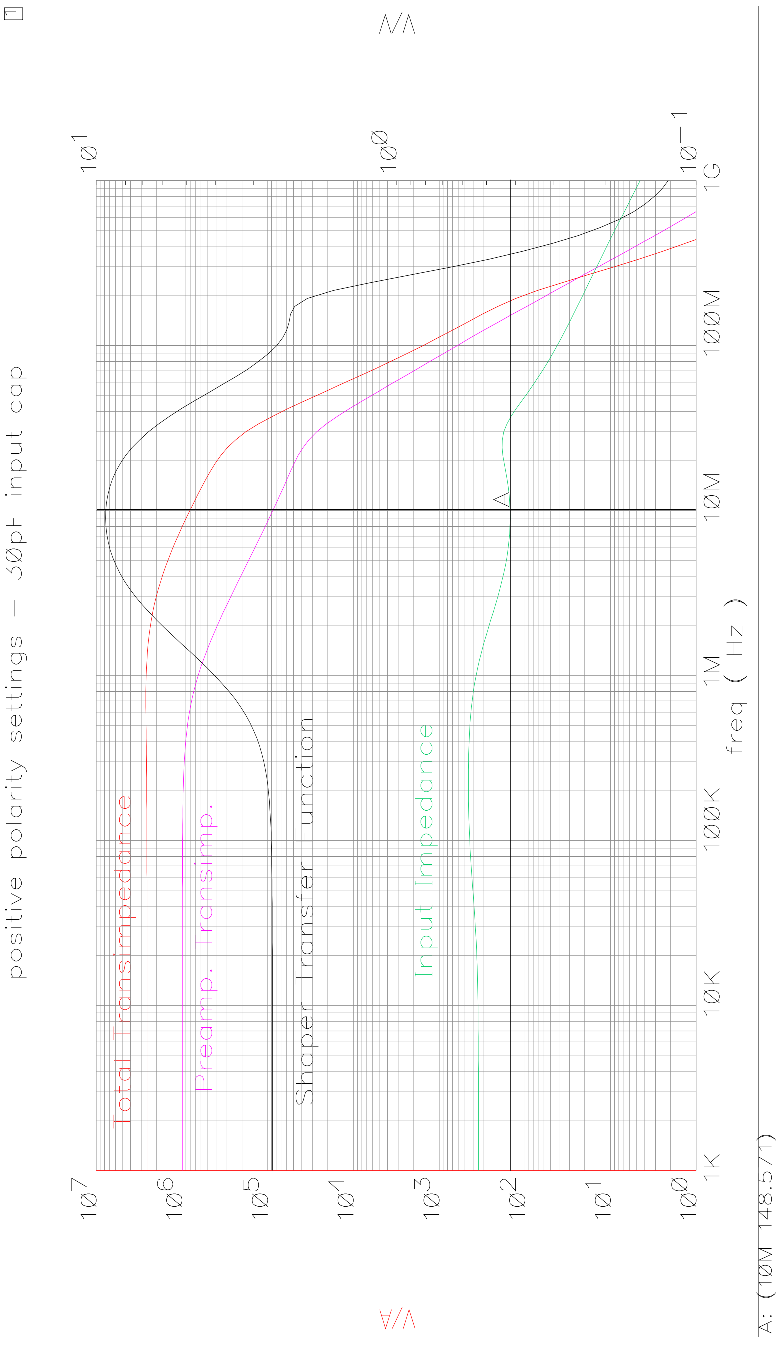

Figure 48: Input Impedence vs. frequency for positive input charge setup

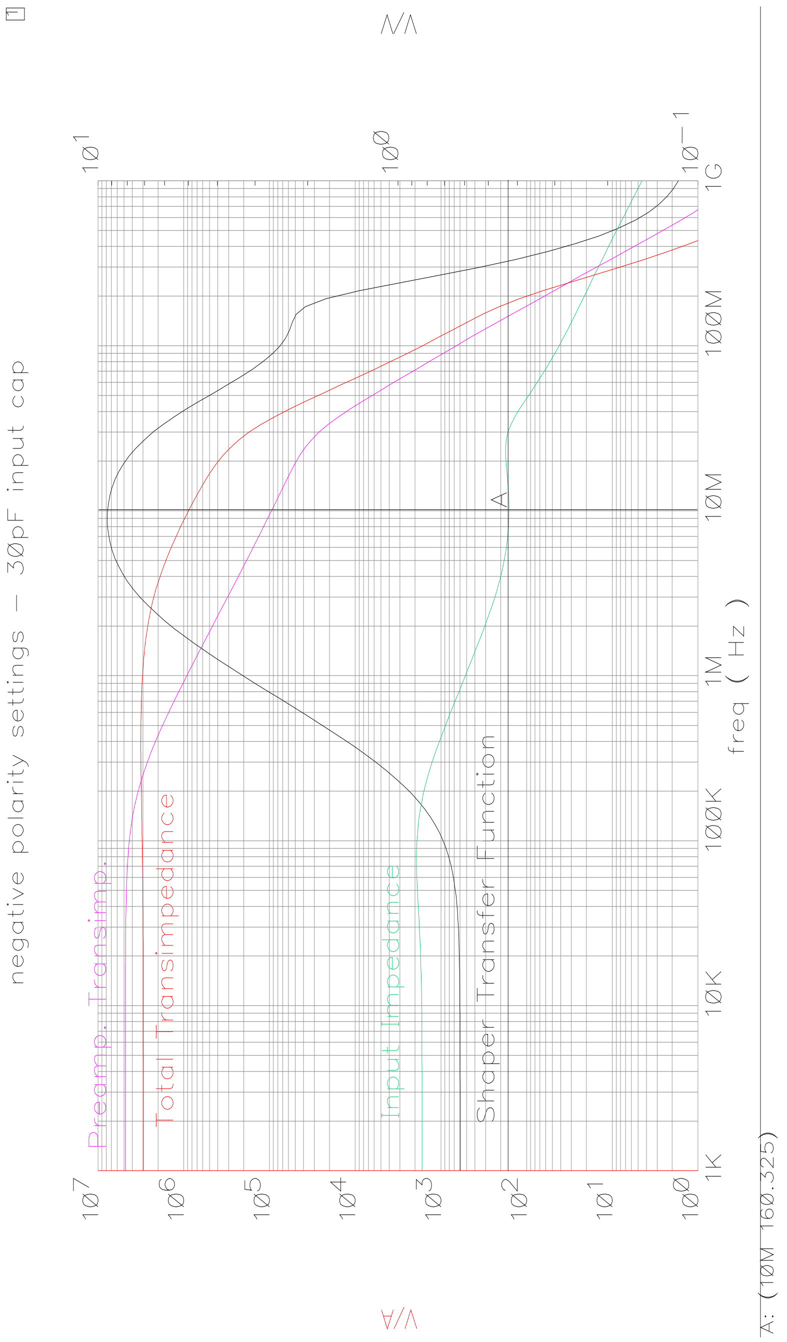

Figure 49: Input Impedence vs. frequency for negative input charge setup

D Test Board

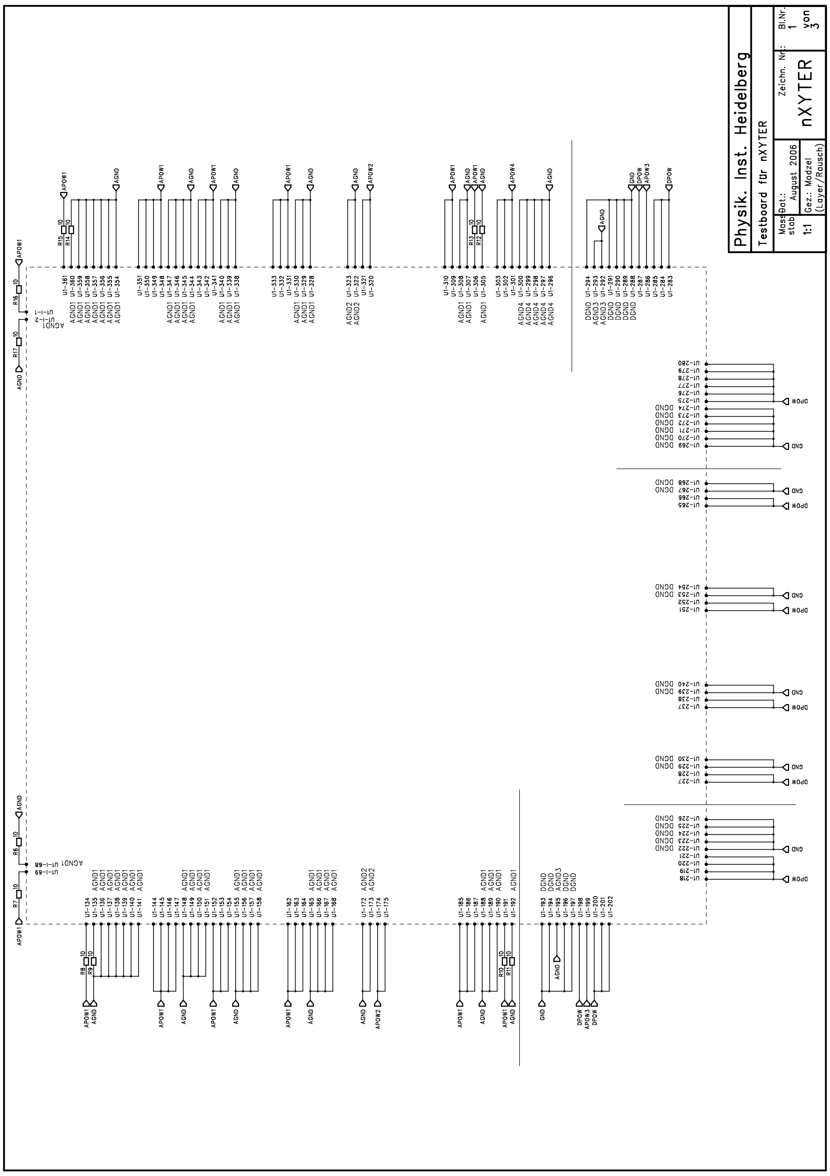

Figure 50: Schematic of the test board (sheet 1 of 3)

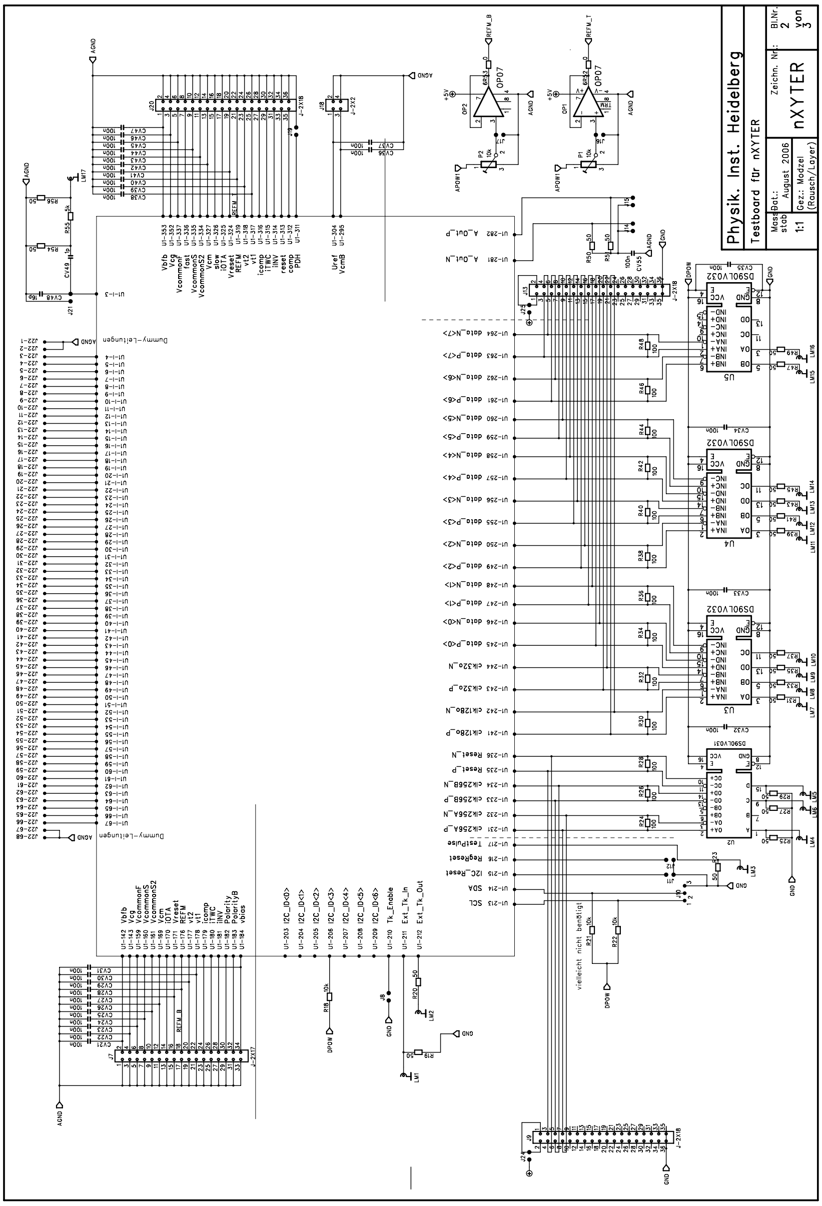

Figure 51: Schematic of the test board (sheet 2 of 3)

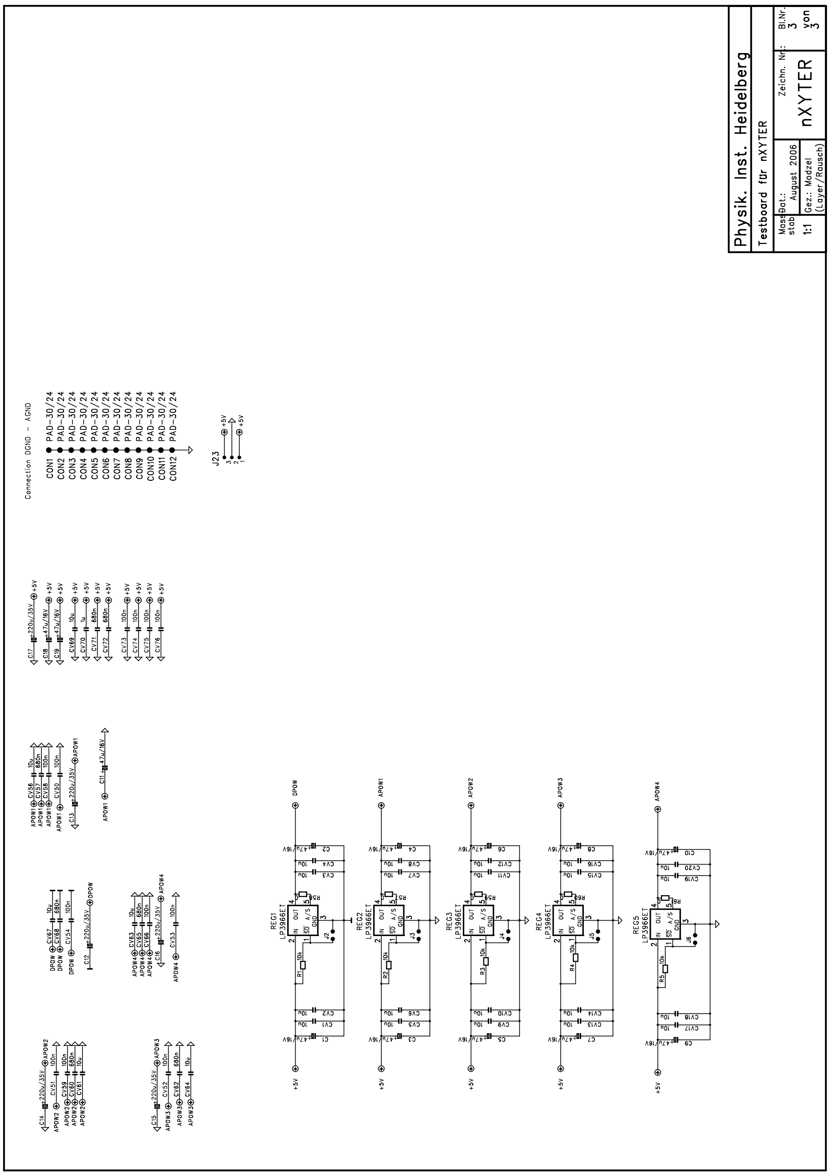

Figure 52: Schematic of the test board (sheet 3 of 3)

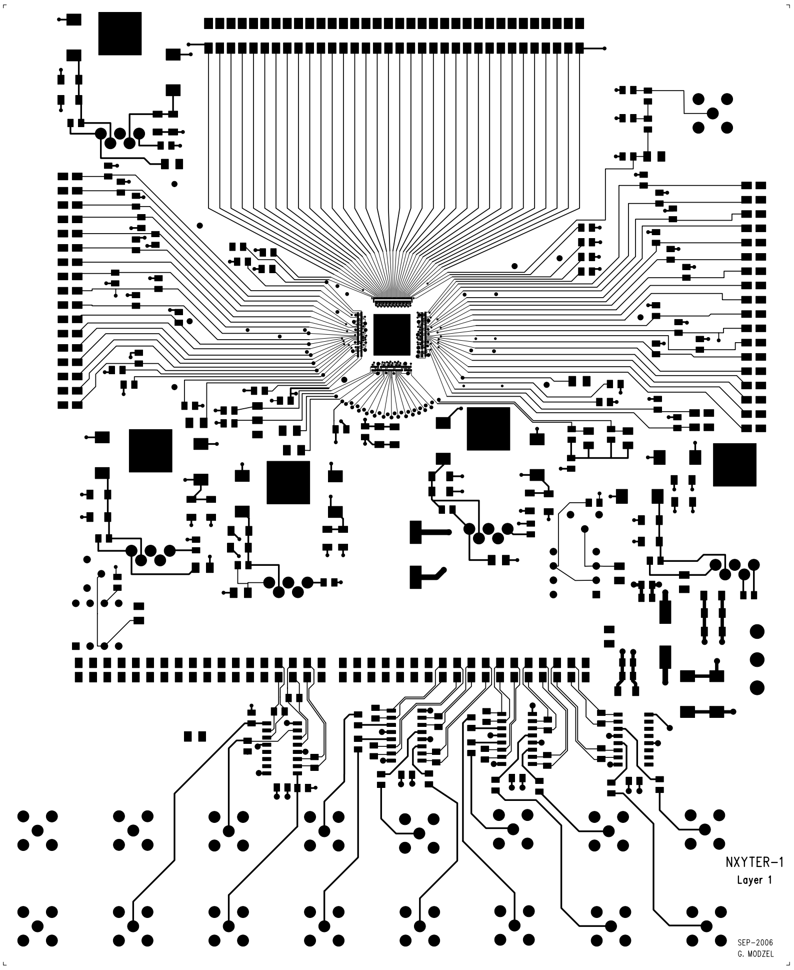

Figure 53: PCB of the test board (layer 1 of 4)

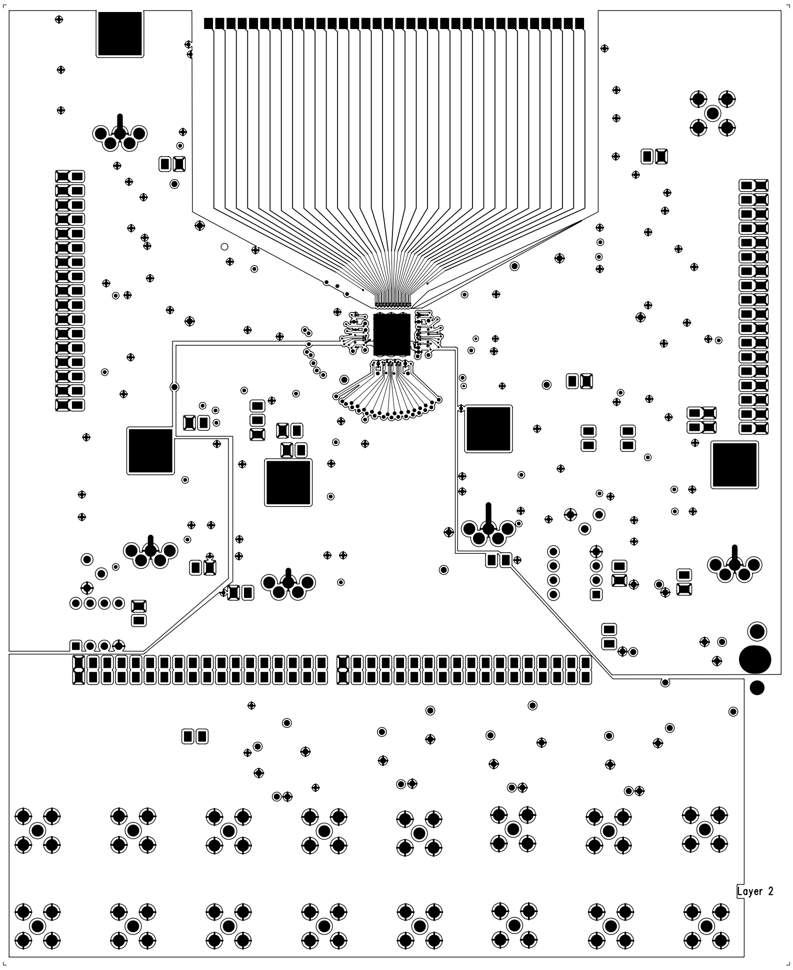

Figure 54: PCB of the test board (layer 2 of 4)

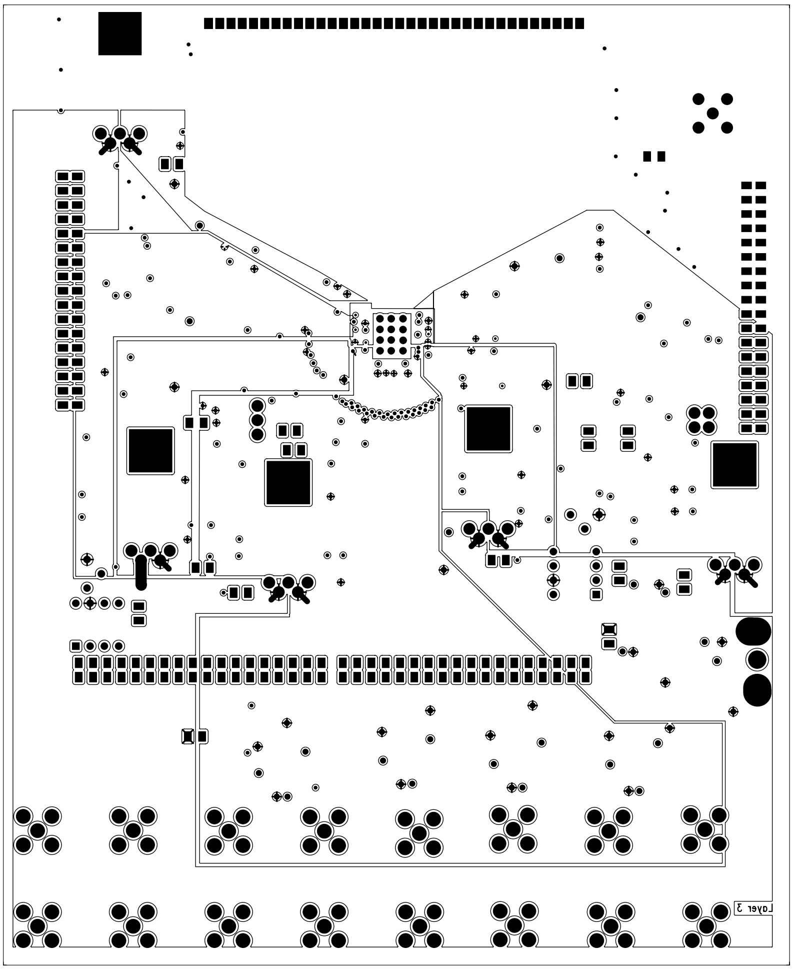

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Figure 55: PCB of the test board (layer 3 of 4)

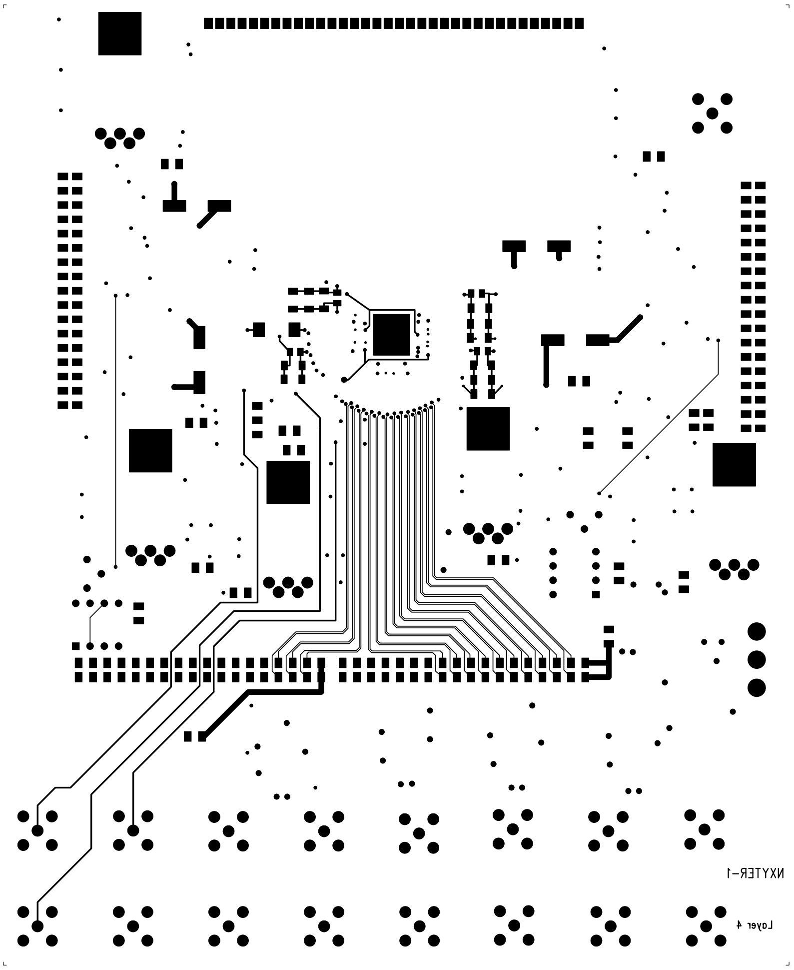

Figure 56: PCB of the test board (layer 4 of 4)

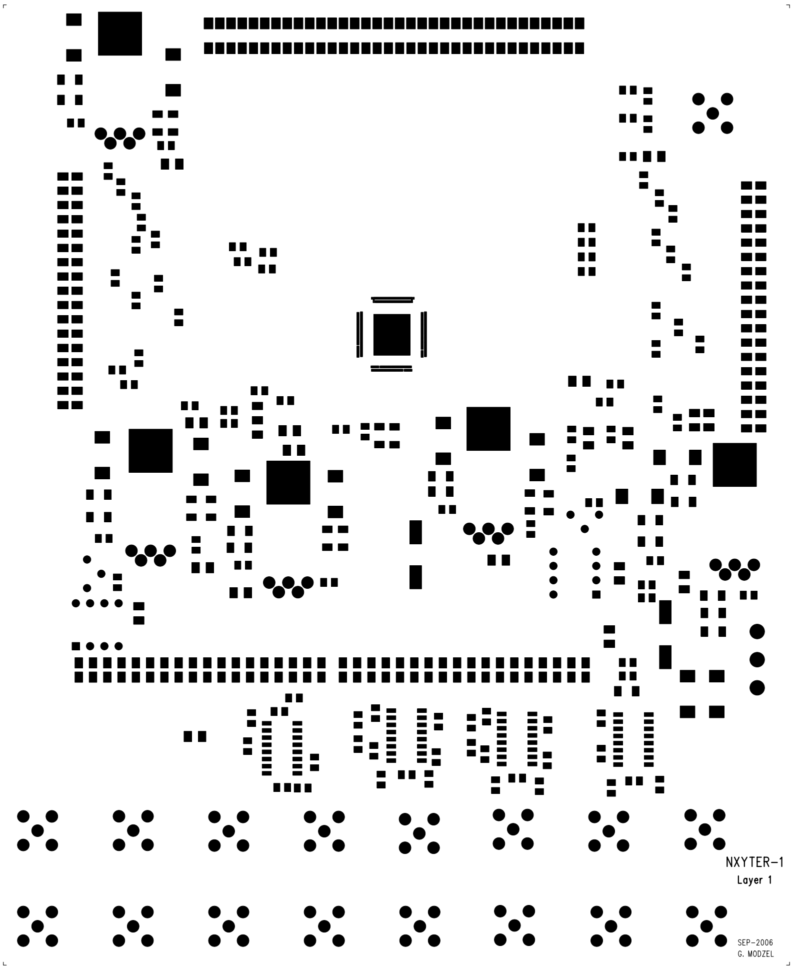

Figure 57: PCB of the test board (solder mask 1 of 2)

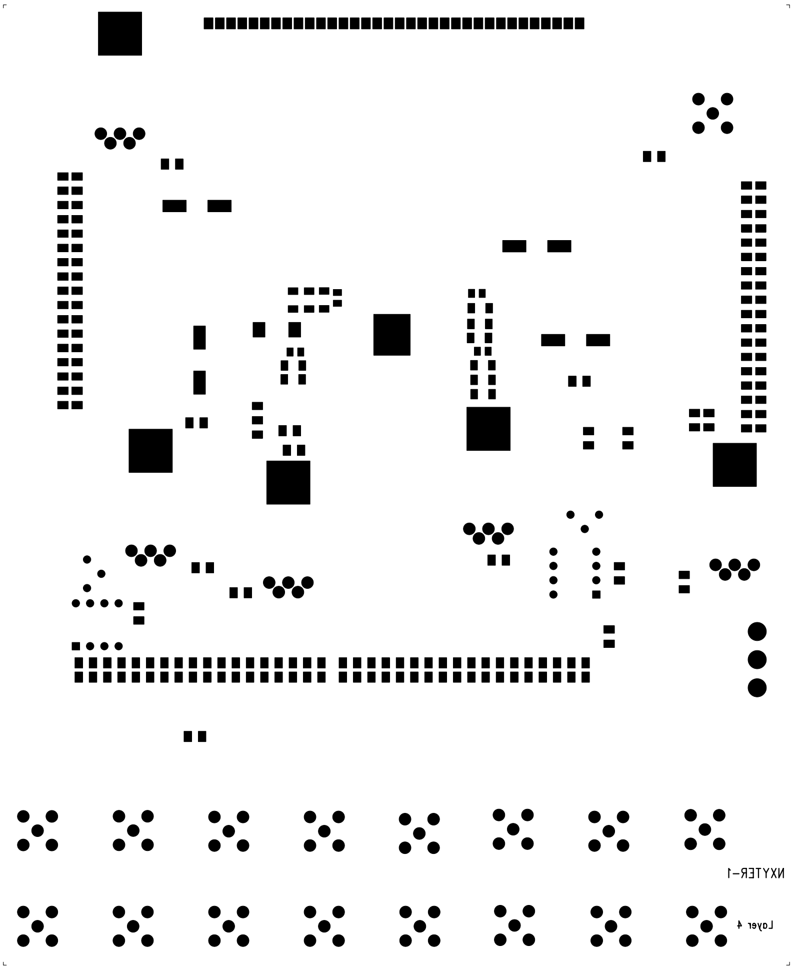

Figure 58: PCB of the test board (solder mask 2 of 2)

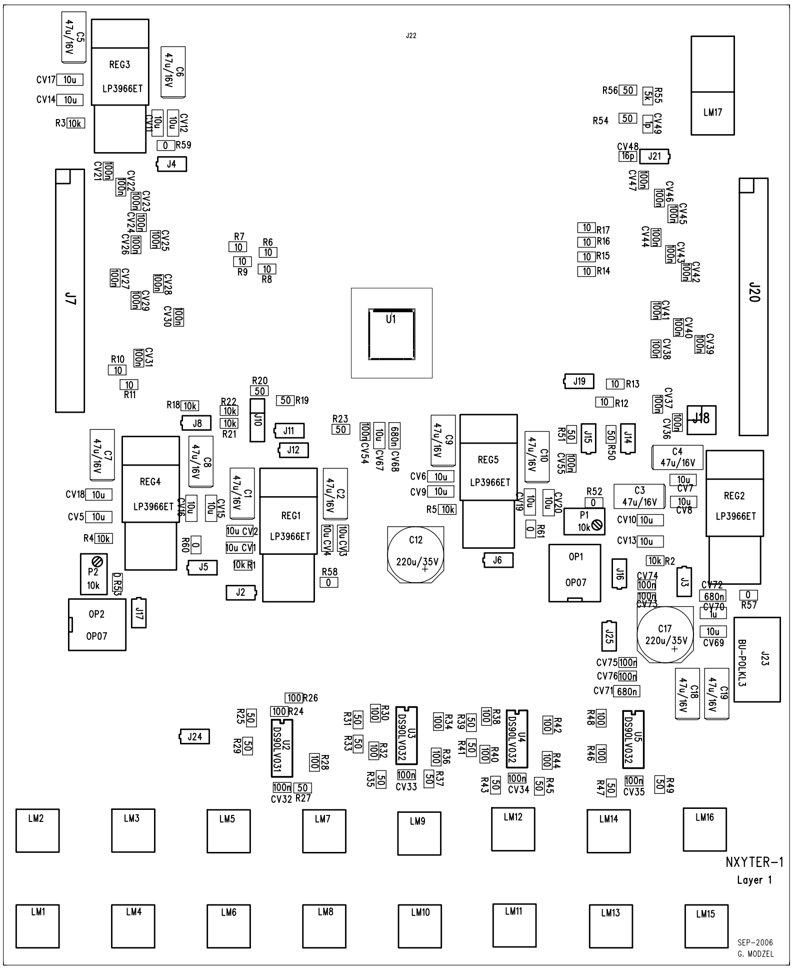

Figure 59: PCB of the test board (components 1 of 2)

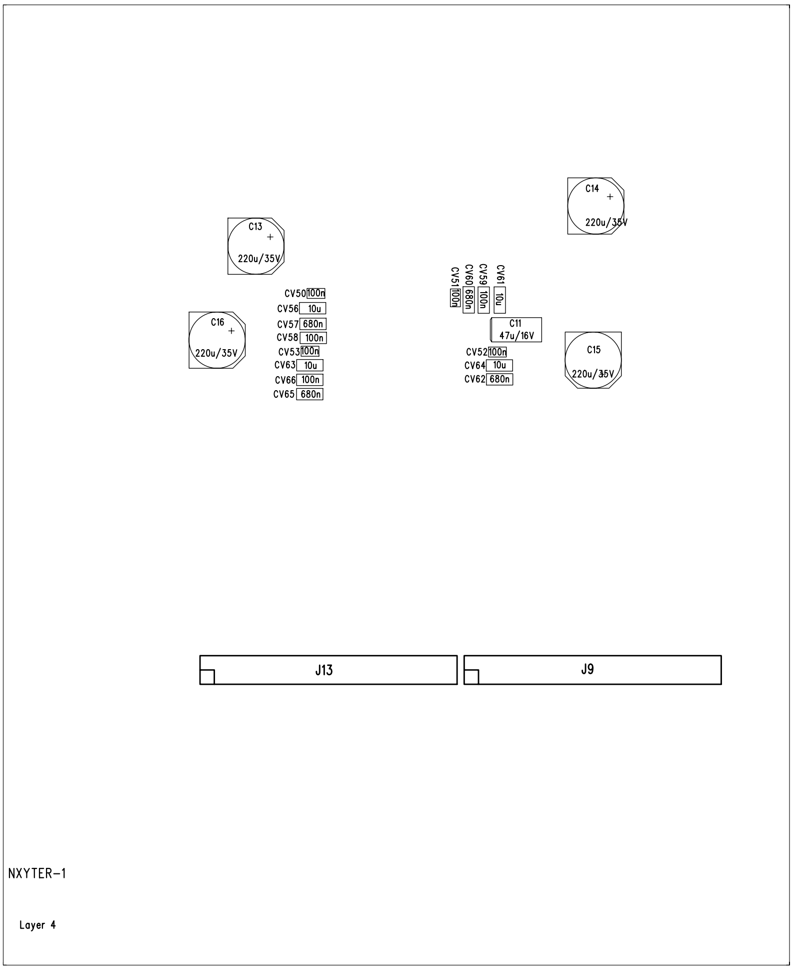

Figure 60: PCB of the test board (components 2 of 2)

E Gray code tables for the output data

Table 18: Correspondence between the TS bits and time-stamp

channel number	TS[13..0] binary gray encoded	TS[13..0] decimal gray encoded
0	00000000000000	(0)
1	00000000000001	(1)
2	00000000000011	(3)
3	00000000000010	(2)
4	00000000000110	(6)
5	00000000000111	(7)
6	00000000000101	(5)
7	00000000000100	(4)
8	00000000001100	(12)
9	00000000001101	(13)
10	00000000001111	(15)
11	00000000001110	(14)
12	00000000001010	(10)
13	00000000001011	(11)
14	00000000001001	(9)
15	00000000001000	(8)
16	00000000011000	(24)
17	00000000011001	(25)
18	00000000011011	(27)
19	00000000011010	(26)
20	00000000011110	(30)
21	00000000011111	(31)
22	00000000011101	(29)
23	00000000011100	(28)
24	00000000010100	(20)
25	00000000010101	(21)
26	00000000010111	(23)
27	00000000010110	(22)
28	00000000010010	(18)
29	00000000010011	(19)
30	00000000010001	(17)
31	00000000010000	(16)
32	00000000110000	(48)
...	...	...
16343	10000000111100	(8252)
16344	10000000110100	(8244)
16345	10000000110101	(8245)
16346	10000000110111	(8247)
16347	10000000110110	(8246)
16348	10000000110010	(8242)
16349	10000000110011	(8243)

Table 18: Correspondence between the TS bits and time-stamp

channel number	TS[13..0] binary gray encoded	TS[13..0] decimal gray encoded
16350	10000000110001	(8241)
16351	10000000110000	(8240)
16352	10000000010000	(8208)
16353	10000000010001	(8209)
16354	10000000010011	(8211)
16355	10000000010010	(8210)
16356	10000000010110	(8214)
16357	10000000010111	(8215)
16358	10000000010101	(8213)
16359	10000000010100	(8212)
16360	10000000011100	(8220)
16361	10000000011101	(8221)
16362	10000000011111	(8223)
16363	10000000011110	(8222)
16364	10000000011010	(8218)
16365	10000000011011	(8219)
16366	10000000011001	(8217)
16367	10000000011000	(8216)
16368	10000000001000	(8200)
16369	10000000001001	(8201)
16370	10000000001011	(8203)
16371	10000000001010	(8202)
16372	10000000001110	(8206)
16373	10000000001111	(8207)
16374	10000000001101	(8205)
16375	10000000001100	(8204)
16376	10000000000100	(8196)
16377	10000000000101	(8197)
16378	10000000000111	(8199)
16379	10000000000110	(8198)
16380	10000000000010	(8194)
16381	10000000000011	(8195)
16382	10000000000001	(8193)
16383	10000000000000	(8192)

Table 19: Correspondence between the ID bits and channel number

channel number	ID[7..0] binary gray encoded	ID[7..0] decimal gray encoded
0	0000000	(0)
1	0000001	(1)

Table 19: Correspondence between the ID bits and channel number

channel number	ID[7..0] binary gray encoded	ID[7..0] decimal gray encoded
2	0000011	(3)
3	0000010	(2)
4	0000110	(6)
5	0000111	(7)
6	0000101	(5)
7	0000100	(4)
8	0001100	(12)
9	0001101	(13)
10	0001111	(15)
11	0001110	(14)
12	0001010	(10)
13	0001011	(11)
14	0001001	(9)
15	0001000	(8)
16	0011000	(24)
17	0011001	(25)
18	0011011	(27)
19	0011010	(26)
20	0011110	(30)
21	0011111	(31)
22	0011101	(29)
23	0011100	(28)
24	0010100	(20)
25	0010101	(21)
26	0010111	(23)
27	0010110	(22)
28	0010010	(18)
29	0010011	(19)
30	0010001	(17)
31	0010000	(16)
32	0110000	(48)
...	...	...
96	1010000	(80)
97	1010001	(81)
98	1010011	(83)
99	1010010	(82)
100	1010110	(86)
101	1010111	(87)
102	1010101	(85)
103	1010100	(84)
104	1011100	(92)
105	1011101	(93)
106	1011111	(95)
107	1011110	(94)

Table 19: Correspondence between the ID bits and channel number

channel number	ID[7..0] binary gray encoded	ID[7..0] decimal gray encoded
108	1011010	(90)
109	1011011	(91)
110	1011001	(89)
111	1011000	(88)
112	1001000	(72)
113	1001001	(73)
114	1001011	(75)
115	1001010	(74)
116	1001110	(78)
117	1001111	(79)
118	1001101	(77)
119	1001100	(76)
120	1000100	(68)
121	1000101	(69)
122	1000111	(71)
123	1000110	(70)
124	1000010	(66)
125	1000011	(67)
126	1000001	(65)
127	1000000	(64)

References

[1] DS90C032, LVDS Quad CMOS Differential Line Receiver, National Semiconductor Corporation, September 22, 2003 (2003) National Semiconductor, DS90C032 LVDS Quad CMOS Differential Line Receiver, June 1998

[2] The I^2C-bus and how to use it, Philips Semiconductors, April 1995 (1995)

[3] Philips Semiconductors, Application Note 97055, “Bidirectional level shifter for I^2C-bus and other systems”, August 4th 1997 (1997)