Radiation tolerance of the Universal Read Out Controller

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Since 2007 our contribution focused on the Silicon Tracker's FEE (Front End Electronic), consisting of the nXYTER, an ADC (Analog Digital Converter) and a ROC (Read Out Controller). Since 2009 we are also designing and implementing readout logic for the GET4 chip [1] and the TRD FEE. To keep the re-usability as high as possible, we split the ROC into two fully independent modules: the readout logic and the transport logic. This modularization of the Read Out Controller and the consequential separation of the control software into different layers, enabled us to provide a Universal ROC, which offers quick access to a long-run tested transport logic and allows us to easily add a new readout logic for further FEE setups [2].

Radiation Tolerance

The heart of the Universal ROC is an SRAM based FPGA, since FPGAs provide the best combination of performance and long-term flexibility. However, there is a crucial problem regarding FPGAs: the radiation which is inevitable in high energy physics experiments can cause the FPGA's doped silicon to change its electrical properties, depending on its Linear Energy Transfer (LET). This physical separation of electron-hole pairs results in spontaneous Single Event Effects (SEE) as well as long-term Total Ionizing Dose (TID) cumulation within the material. SEEs, especially Single Event Upsets (SEU) and Single Event Transients (SET), show up as permanent, but non-destructive binary bit flips within logic memory or as short glitches on the routing network. This becomes extremely critical for latches or flip-flops at clock signal setup/hold times. TID effects are not that critical for short-term applications, but preponderantly problematic for long-term considerations. They increase the number of stuck charges resulting of the electron-hole pair separation, leading to modification of the chips doped semiconductor properties. Overall, hardware failures may occur in nonrelevant circuits or may lead to spontaneous unexpected system behavior, but most critical they can lead to a total system halt, known as Single Event Functional Interrupt (SEFI) [3].

According to this problem, very specialized shielded radiation hard materials have been and currently are developed for military and space grade FPGAs, realized within the Xilinx Virtex QPro II, 4 and 5 series, complemented by a configuration refresh feature called "scrubbing". As some of these chips are not available for commercial applications due to military export restrictions, common devices are provided with special TID mitigation techniques and SEE failsafe combinations of logic blocks. Basically, such ambitions in securing the logical hardware design layer can be realized by three different approaches: spatial redundancy, temporal redundancy and various combinations of both. Spatial redundancy features synchronous data sampling of combinational logic at multiple routes to mitigate SEUs. The addition of adjacent voters is required to analyze processed data values. Well known candidates using this principle are Dual and Triple Modular Redundancy (DMR/TMR), mostly accompanied by Error Detection and Correction Codes (EDAC). Temporal redundancy enables a single combinational logic circuit to be sampled at multiple times. Additional voter circuitry compares all of the results and decides whether an error occurred or not. The combination of both spatial and temporal redundancy leads to SEU and SET immunity.

Conclusions

The usability of FPGAs in radiation environments highly depends on the usage of mitigation technologies such as scrubbing, spatial or temporal redundancy. This has a strong influence on the board design as well as on the FPGA design: the Universal ROC is implemented on a board (namely the SysCore Board) which provides an external FLASH memory and an additional radiation hard flash-based FPGA which are required to realize the scrubbing technology [4]. Furthermore the modules (transport logic as well as readout logic) are using a combination of spatial and temporal redundancy. The implemented architecture layers and methods have been practically tested under experimental conditions within different particle accelerator beams. The Universal ROC had been directly placed into the center of the particle beam line to get comprehensible results at a maximum ionization impact. These tests will be continued in 2011 and will be used to develop a radiation tolerant Universal ROC.

References

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