CBM-TRD readout with the SPADIC amplifier / digitizer chip

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The SPADIC chip is being developed for the readout of the CBM Transition Radiation Detectors (TRD). The basic readout concept is to perform both the amplification and the digitization of the (charge) pulses from the CBM TRD in a single front-end ASIC. It is intended to continuously digitize the whole shaper pulses which allows for a flexible subsequent feature extraction (amplitude, time, etc.) either directly on the chip or in some FPGA (both options are currently subject of discussion). The group in Heidelberg started the development of the SPADIC (Self triggered Pulse Amplification and Digitization asIC) chip in 2008. The latest prototype SPADIC 0.3 contains 26 channels with input protection and different amplifier versions, out of which 8 are equipped with pipelined 9 Bit ADCs running at 25 MHz.

The system noise including the ADC was measured to $\approx 800\,\mathrm{e}^-$ at a peaking time of 80 ns and a capacitive input load of 30 pF while consuming 3.6 mW for the front-end and 4.5 mW for the ADC per channel. Using static input signals the resolution of the ADC is close to 8 Bit (INL slightly larger than 0.5 LSB).

The prototype chip also contains an on-chip digital memory which can record snapshots of up to 42 ADC data samples that can be read out later at slower speed. The architecture is self-triggered so that an amplitude above a programmable threshold triggers data storage on a per channel basis.

The final chip will also include a digital IIR filter to eliminate long ion tails as well as a fast serial interface compatible to the CBM DAQ data format. With the help of measured detector pulses the optimal filter structure (filter order, topology, word widths, etc.) is presently being evaluated. A first iteraton of the filter will already be realized in the next ASIC prototype. A web page about the SPADIC chip has been created at `http://spadic.uni-hd.de`.

In order to read out several SPADIC chips when mounted on the test chambers, a versatile fast data acquisition board and a suited SPADIC interface board (see Fig. 1) were developed and tested. The SUSIBO ('SuS Interface BOard') contains a USB 2.0 interface, a large Xilinx FPGA, memory, Ethernet IO and a differential interface to the trigger logic. It is controlled by custom software running under Linux. The interface board houses a SPADIC chip (wire bonded to the PCB), interface and biasing circuitry and a ZIF connector to connect TRD chamber prototypes to the amplifier inputs. Eight units have been assembled for use mainly in the 2010 TRD beam test. A 2^{nd} generation interface board with improved interfacing and better signal routing is presently being prepared.

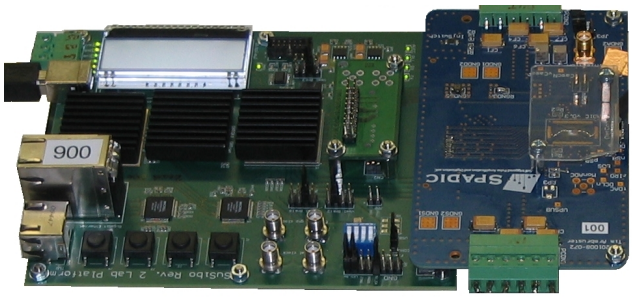

Figure 1: SUSIBO readout board (left) and interface board with SPADIC chip (right)

The readout system was successfully used in the 2010 CBM test beam campaign at CERN to read out TRD prototype detectors from Frankfurt and Münster. A screen shot of the online event display with two detector pulses is shown in Fig. 2. The data are presently being analyzed.

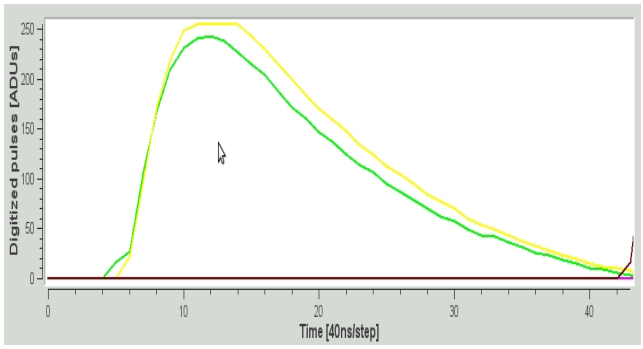

Figure 2: Online display of detector pulses digitized with the SPADIC chip (Self triggered Pulse Amplification and Digitization asIC)