Development of a data-driven readout ASIC for microstrip detectors

E. Atkin, Yu. Bocharov, V. Butuzov, A. Klyuev, D. Osipov, V. Shumikhin, A. Simakov, and A. Voronin
National Research Nuclear University "MEPhI", Moscow

We present the current status of the development of an asynchronous data-driven architecture for multichannel silicon tracker system experiments. The known event statistics in multichannel equipment permits to use new variants of architecture synthesis with the use of analog de-randomizing blocks. The requirements of the silicon tracking system of the CBM experiment were used in the design.

The ASIC with analog de-randomization, which has been under development for the last few years, consists of two parts: the front-end readout and the data processing ones. The readout chain contains a charge-sensitive amplifier, followed by shaper and comparator. The data processing channel includes a peak detector and an ADC (one for all the channels for this prototype run). The block diagram was presented in [1, 2, 3]; a more detailed description is given in [4].

The functionality of de-randomization of analog signals is provided by an analog key array, managed by a logical unit that can analyze the random appearance of the input signals in the readout channels and the possibility of their transfer to the free processing channels. The logic of the de-randomizer is based on the fact that the pulse shape is known, and the fact that the number of processing channels is chosen such that the number of occupied readout channels equals the number of processing channels under maximum load, and at maximum load, the average hit period in a channel equals the processing time of a hit. To avoid distortion of the amplitude information, it is necessary to switch all channels in a time not exceeding a certain peaking time of the signal. Given that every act of switching the readout channel to a processing one occurs at the front of a clocking signal, it is sufficient to establish its frequency such that the duration of a number of cycles equal to the number of processing channels will be less than the peaking time of the input signals.

The basic task in 2010 was to develop a prototype version of the de-randomizing ASIC and to implement a high-speed analog switching circuit of the 128 to 16 structure. One of the aims for the design was to improve the arbitration logic used and supplement the ASIC by both an input analog part and an output ADC. The principal feature of the ASIC is a low power consumption – within 2 mW/channel at a maximum average channel hit-rate not less then 150 kHz.

The analog part includes a DC CSA with a circuit of detector leakage current compensation (up to 1 μA) and a CR-RC shaper (100 ns peaking time), both designed according to the STS specifications [5]. The de-randomizing part consists of an asymmetrical analog switch array and arbitration logic. The number of readout chains was reduced down to 24 and provides a cost-effective approach at prototyping. The ASIC was manufactured using the UMC 0.18 μm CMOS process. The ASIC layout is shown in Fig. 1; its area occupied on chip is 1525×3240 μm^2 (double mini-asic). The chips were encapsulated in PGA144 cases, and a test setup is being developed.

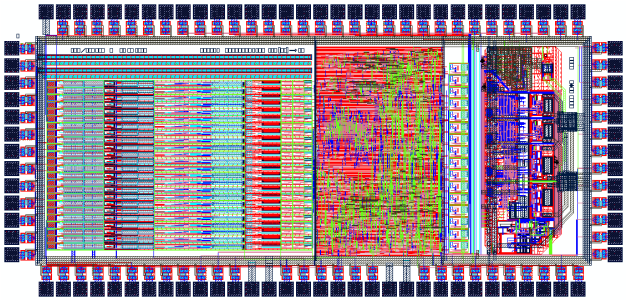

Figure 1: The ASIC layout

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References

[1] E. Atkin *et al.*, *CBM Progress Report 2009*, Darmstadt 2010, p. 45

[2] E. Atkin *et al.*, Instrum. Exp. Tech. **53** (2010) 524

[3] E. Atkin *et al.*, *Development of the data-driven readout ASIC for microstrip detectors*, Proc. IEEE EWDTS, St. Petersburg (2010), p. 374

[4] A. Klyuev, Ph.D. thesis, MEPhI, Moscow, 2010

[5] E. Atkin *et al.*, Instrum. Exp. Tech. **53** (2010) 520