Front-end electronics for high counting rate TRD

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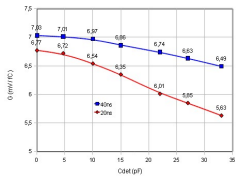
Fast Analog Signal Processor FASP-0.1 [1, 2] is a prototype ASIC designed at NIPNE for HCR-TRD having in mind the CBM experiment at FAIR. In this contribution we report on relevant measured parameters of ASIC analog channels and a FEE based on FASP, designed and built for in-beam tests of our HCR-TRD prototypes [3].

The measured ASIC parameters [4, 5] are:
- quiescent supply current (V_D = 3.3V): 30mA $\pm$1mA.
- output baseline shift :
  - with power supply (V_D = 3.0- 3.6V): $< 0.07\%$;
  - with detector leakage current (I_L=$\pm$ 50nA): $<9\mu$V/nA.
- conversion gain G vs. C_{det} (for FAST outputs):



Gain slope:
0.50% for τ = 20 ns
0.23% for τ = 40 ns

Figure 1: Conversion gain G vs. C_{det}

- integral nonliniarity (INL)(0-1V linear range):
INL = 1.0% for τ =20ns, FLAT output;
INL = 0.2% for τ =40ns, FAST output.
- overload recovery (for FAST outputs, τ = 40 ns): first pulse: x10 overload ; second pulse: after 400ns (corresponding average pulse rate $>$ 300kcps).

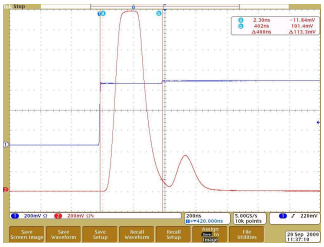
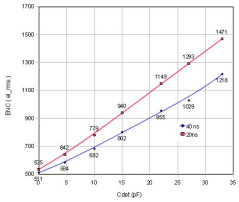


Figure 2: Overload recovery

- electronic noise charge ENC vs. C_{det} for FAST outputs:



Noise slope vs. shaping time:

30.0 e/pF for τ = 20 ns
23.3 e/pF for τ = 40 ns

Figure 3: ENC vs. C_{det}

Front End Electronics (FEE) was designed to cope with the requirements for in-beam test of 3 different HCR-TRD prototypes. The requirements are:
- acceptable immunity to the "pick-up" noise;
- long transmission line of detector signals to ADC;
- NIM logic standard for request/grant protocol;
- 16 analog signal channels for each detector (48 total).
FEE is splitted in two units (Fig.4). The first one, motherboard, houses one FASP ASIC for wich it provides power supply, all DC references voltages (THRESHOLD, BASELINE,etc.), 8 analog buffers with differential outputs (each buffer can be switched to handle FAST or FLAT TOP signal), and NIM logic standard interface (EVT, REQ, RDY, RST signals). Motherboard is a three layers PCB of 100x120mm^2 size. The second one, adapter board, has two identic sections. Each section has 8 differential input channels providing single-ended outputs. DC output levels can be adjusted to match ADC inputs. Adapter board is three layers PCB of 78x74mm^2 size.

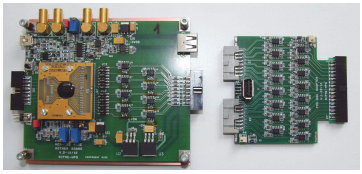


Figure 4: ASIC MB (Left) and Adapter(Right)

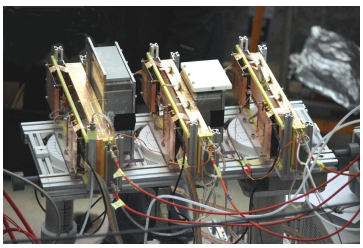


Figure 5: Experimental set-up used in the in-beam test

HCR-TRD prototypes, the described FEE (48 channels) and geometry control mechanism (Fig.5) were succesfully tested at T10 beam line of the CERN PS accelerator, last November .

References

[1] V.Catanescu, CBM 10th Colaboration Meeting, Sept. 25-28,2007, Dresden
[2] V.Catanescu, et al., DPG,Bochum, March 18,2009
[3] M.Petris et al., contribution to this Sci.Rep.
[4] A. Caragheorgheopol et al., 14th CBM Colaboration Meeting, Split,Oct.6-9,2009.
[5] A. Caragheorgheopol et al., CBM FEE/DAQ Workshop, Feb. 22-23,2010,GSI