Evolution of a prototype Silicon strip detector readout ASIC for the STS

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The TOT01 prototype readout ASIC for the CBM STS detector was manufactured and tested in 2010. Its purpose was to test the usability of the time-over-threshold method in this application [1]. The tests revealed a significant potential of the TOT architecture. It is able to provide a low-noise, low-power and simple solution for energy measurement [2]. Since it is possible to smoothly adjust the chip's noise vs. speed characteristic to meet the application-specific requirements, its performance was evaluated for two arbitrary, opposite settings called "fast" and "slow". The performance of the TOT01 ASIC is summarized in Table 1.

GBW	1.2 GHz	power/ch	1.2 mW
gain	1600 [V/V]	$ENC^{Cdet=28pF}_{fast}$	700 e^-
CSA gain	$\approx$ 13 mV/fC	$ENC^{Cdet=4pF}_{slow}$	162 e^-

Table 1: Performance of the TOT01 ASIC

TOT02, an upgraded version of this ASIC (Fig. 1) , was submitted, fabricated and preliminarily tested. The chip consists of 16 channels, improved ToT-based CSA and discriminator in a radiation-hard layout and a digital back-end.

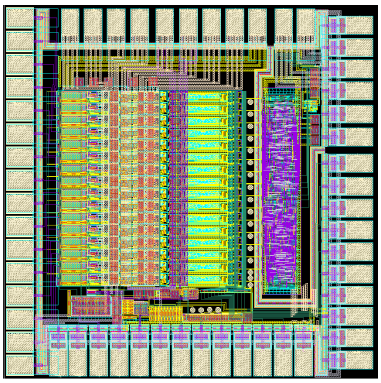

Figure 1: TOT02 ASIC layout

The analogue part contains enhanced charge-sensitive amplifier (CSA) architecture (folded cascode with booster) and modified constant-current, complementary discharge circuits (Fig.2). These changes were to minimize the pulse tail, which for lower threshold caused deterioration in energy resolution. The CSA is followed by a discriminator supplied with a 6-bit DAC for the DC level spread correction. The pulse stretchers added between the discriminator and the digital back-end prevent from short glitches which could corrupt the operation of the latches. The digital back-end implements timestamp latches triggered by the discriminator output pulse edges, token ring and serializer (Fig. 3). Each channel is supplied with two latches triggered by the consecutive edges of the discriminator. The timestamp value latched first is the event time, while the difference between two latches represents the pulse length and should directly translate to the deposited energy.

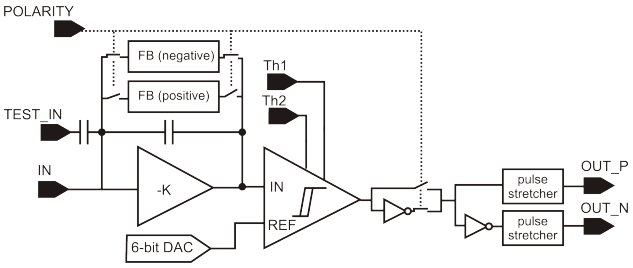

Figure 2: Analog part of the ASIC channel

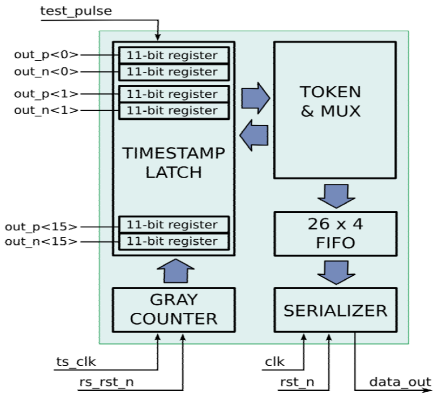

Figure 3: Digital back-end

The test setup of the TOT02 ASIC consists of the main test board incorporating an independent power supply and biasing circuitry with many debugging features. The board supports both direct detector placement and remote detector connection through an ERNI connector (standard connector for STS detectors). The configuration and read-out is performed by a National Instruments DAQ card interfaced to the ASIC through fast level translators for read-out and shift registers for slow control. The tests are ongoing; we expect to receive results soon.

References

[1] K. Kasinski and R. Szczygiel, *CBM Progress Report 2009*, Darmstadt 2010, p. 44

[2] K. Kasinski, R. Szczygiel and P. Gryboś, 2011 JINST 6 C01026