Demonstrator beam time results for the clock distribution and synchronization of the CBM-DAQ system

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Because of new requirements for the DAQ system, the previously planned hierarchical CBM network structure using Read-Out Controllers (ROC) for detector readout, Data Combiner Boards (DCB) for data combining and Active Buffer Boards (ABB) for data buffering and First Level Event Selection (FLES) attachment was extended. The usage of a unified link for three different data types such as Data Transport Messages (DTM), Detector Control Messages (DCM), and Deterministic Latency Messages (DLM) and the communication principles and packet structures will not be changed, because it has proven its reliability [1, 2]. But new detector readout chips and high-level data flow handling concepts generated new feature requests. Therefore, a new CBMnet V2.0 was designed and will be implemented supporting lane handling with different bandwidth in up- and down-link direction, large messages, an adapted data loss strategy in cases of overloads, easy meta data detection, and a fully reliable communication for data streams. The new planned CBM network structure using the CBMnet V2.0 is shown in Fig. 1. The detector readout ASICs can now be connected to the CBM network via a HUB ASIC which provides data aggregation and rate conversion and drives the opto-converter boards. Within the inner network part, the DCB was replaced by a Data Processing Board (DPB), which serves also as a bridge to the Experiment Central System (ECS). The back-end part using ABBs attached to FLES within computing clusters will stay the same. For the HUB ASIC chip and the opto-converter, the analysis and conception has already started; its implementations will be major parts within future work packages.

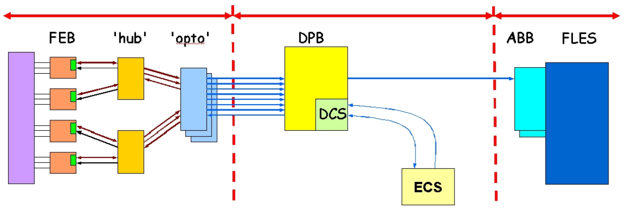

Figure 1: The planned CBM network structure

For the proof of concept and to enable the readout over optics for the detectors used during beam time, a readout chain consisting of the previously developed prototypes was created. The demonstrator build-up used during the beam time tests in December 2010 is presented in Fig. 2. It shows the two DCBs used as DPB prototypes. They were connected to an ABB that served as emulation for the ECS providing the clock and a system synchronization with DLMs via the CBM protocol V1. Both DCBs have four bidirectional connections to the front-end for attachment of four ROCs using the unified CBM protocol for synchronization and data acquisition. The received data is combined to a single data stream within the DCBs and sent to an ABB plugged into a workstation running the current version of the DABC software for data collection. During the complete COSY test beam time from 13th to 19th December, the optical readout demonstrator was used. The data acquisition ran problem-free. The ECS emulation providing the control system and the clock distribution was reliable. The network synchronization worked without errors and delivered the targeted bit-clock synchronization, so that a synchronization with less than 400 ps was guaranteed. The concept of using the unified link providing DLMs for synchronization has now shown its valuable improvement for future detector system solutions.

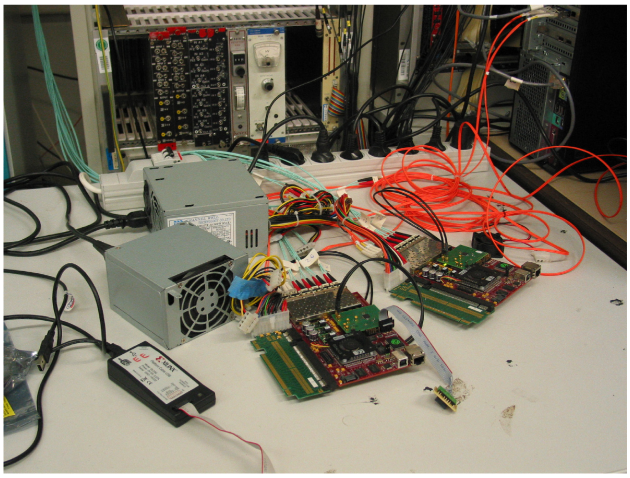

Figure 2: DCBs used in the demonstrator build-up

References

[1] F. Lemke, S. Manz and W. Goa, *Time synchronization and measurements of a hierarchical DAQ network*, Spring meeting of the Deutsche Physikalische Gesellschaft, Bonn, Germany, March 15-19, 2010

[2] F. Lemke *et al.*, *A Unified DAQ Interconnection Network with Precise Time Synchronization*, IEEE Trans. Nucl. Sci. **57**, No. 2 (2010)