Development of PCBs for readout plane and front-end boards for MuCH

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The MuCH layout consists of 18 layers with 6 stations. Simulations suggested that a pad size of 4×4 mm^2 for stations 2 and 3 gives a reasonable performance. In this respect we designed PCBs of 4×4 mm^2 and 3×3 mm^2 pad size. For flexibility and easier fabrication of the readout PCBs, we considered a modular design which can be easily extended to larger PCBs. The basic building block as shown in Fig. 1 consists of an array of 32×8 pads (total 256 pads), and this can be extended to an array of $32 \times 32 = 1024$ pads by multiplicating the basic block. The small pad size imposes severe restrictions on track widths, track-to-track distances and track-to-pad distances. The design and fabrication of such a small pad size cannot be carried out with the conventional approach of using a multilayer PCB with through hole vias only. Hence the design is done using a four-layer PCB with blind vias along with through holes. The signals from all 256 pads are brought to a 300-pin connector (SMT) with 1.27 mm pitch by using blind vias and tracks drawn through inner layers. The blind vias also help in ensuring a gas tight design. The 300-pin female connector on the detector PCB mates with another 300-pin male connector on a 2-chip front-end board (FEB). This FEB processes all 256 analog signals with two nXYTER chips, each processing 128 signals.

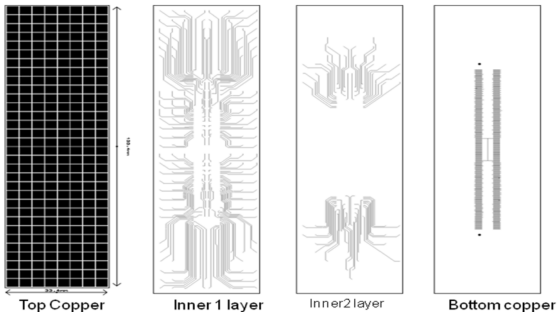

Figure 1: Basic building block for the 32×8 array

For 1024 channels, four specimen of the 2-chip FEB have to be fit into the size of the MuCh PCB, which poses immense size restrictions on the front-end PCB. This led to a PCB design with extremely thin track widths (3 mil), track to track distances as low as 3 mil, and final via sizes like 12 mil. Taking into account all these design restrictions, a prototype PCB was designed. All digital signals to the readout controller (ROC) are connected using a 80-pin connector placed on top copper. The PCB design was done on eight layers, extensively using blind vias on the top and bottom planes. The size of the front-end PCB is 112 mm $\times$ 31 mm as shown in the right panel of Fig 2. The fabrication for this design is in process.

Figure 2 shows the schematic of the proposed readout PCB with 4×4 mm^2 pads in a 32×32 array (1024 channels). All 1024 channels will be read by four FEBs. The left panel shows the top layer with pads while the right panel shows the bottom layer with four 300-pin connectors along with the proposed two-chip FEB boards. The inner layers are not shown.

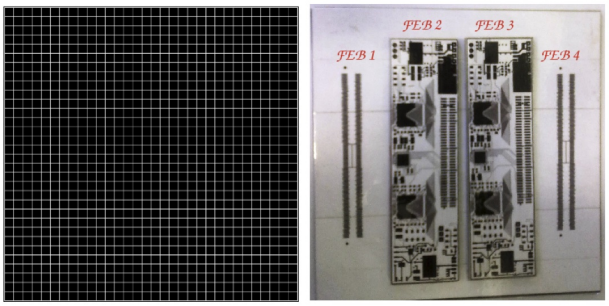

Figure 2: One readout module with 1024 channels. Left: Top view with 4×4 mm^2 pads. Right: Bottom view with connectors and two connected FEBs.

As a first attempt towards fabricating multilayer padplane PCBs with blind vias for readout, two 512-channel PCBs with pad sizes 3×3 mm^2 and 4×4 mm^2 were prepared. A GND plane between each track was introduced in order to reduce the crosstalk between two nearby channels. These PCBs were used in the COSY test beam in December 2010.

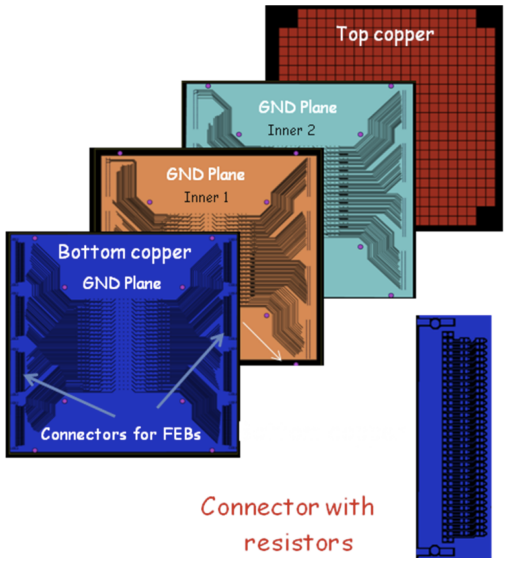

Figure 3: Layout of PCB used in the test beam at COSY