Status of the CBM-MVD prototype readout

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The readout system of the prototype of the CBM-MVD is intended to form a flexible software and hardware solution, which provides the bandwidth and scalability needed for a use in the final MVD. It will be developed based on the state-of-the-art prototype sensor MIMOSA-26 [1]. Despite the readout speed of this sensor not yet being optimised for the final MVD, MIMOSA-26 provides already today the full architecture foreseen for the final MVD and may therefore serve as a useful model of the final sensor.

The MIMOSA-26 sensor handles 570 hits per frame and provides a digital output data stream of 160 Mbit/s sent via two digital output lines. The data stream holds addresses of the pixels containing hits, and frame numbers. A firmware update of our MAPS readout board allowed us to read out the MIMOSA-26 sensors. Furthermore, we were able to reduce the data stream to 80 Mbit/s by removing redundant information.

The future sensors equipping the first generation CBM-MVD will presumably handle a several times higher occupancy than MIMOSA-26, likely ranging up to 800 Mbit/s [2].

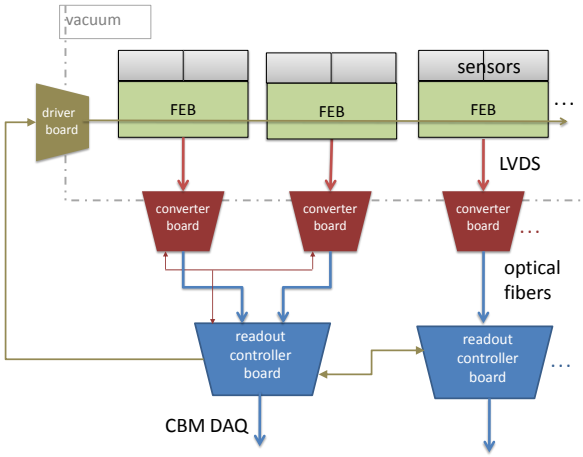

Figure 1: The prototype readout chain

The concept of the readout system of the MVD-prototype is designed accordingly. Figure 1 shows a sketch of the envisaged architecture of the prototype readout chain. Two sensors will be bonded on a flex-print cable, which transfers the data via a fine pitch connector to a front-end board. The future radiation environment requires the use of a radiation-tolerant, passive board. This board serves as an interface between the flex-print cables and conventional copper wires. Moreover, it distributes the sensor clock and the slow-control signals. The data of the two digital output channels of each sensor are transferred via LVDS cables to a converter board. Currently we consider two functionalities for this board. By embedding it into a vacuum flange, we aim to use the board to pass the cables out of the vacuum of the combined MVD and target chamber. The second task is the data conversion from LVDS to 8 bit/10 bit encoded, 1 Gbit/s, optical signals (see Fig. 2 for details).

A readout controller board receives the optical signals. It hosts an FPGA which controls the data acquisition and allows using on-line data reduction and filtering algorithms.

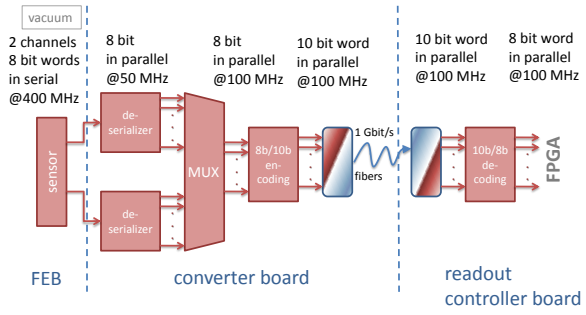

Figure 2: Data flow with the different conversion steps

Slow control will be done by JTAG boundary scan which allows accessing the internal register of the individual sensors. The slow control ensures also latch-up handling and monitoring of on-line temperature and current.

The boards are submitted for production and will be assembled and tested in the next months. In parallel to the hardware developments, the related FPGA firmware is being developed.

References

[1] C. Hu-Guo *et al.*, Nucl. Instr. Meth. Phys. Res. **A 623** (2010) 480

[2] S. Seddiki *et al.*, *Expected data rates of the CBM-MVD at SIS-100 based on realistic beam intensity fluctuations*, this report