Memory kernel development of the Active Buffer

A. Wurz, W. Gao, A. Kugel, and A. Männer
Informatik V, ZITI, University of Heidelberg, Germany

Originally the Active Buffer Board (ABB) for the CBM experiment used an elasticity buffer based on the internal RAM blocks of the Xilinx FPGA, limiting the size to 128 kB. To increase the size of the buffer we completed in 2010 the large-size DDR2 SDRAM FIFO project on the AVNET Virtex5 board [1]. An additional data count module was added and verified. The buffer has been used during last beam tests and worked properly.

Block diagram

We use a 64-bit DDR2 SDRAM module of 256 MB as kernel memory. Figure 1 shows the block diagram of the large-size FIFO. The DDR2 SDRAM module is outside the FPGA. Inside the FPGA we use two smaller built-in FIFOs, 4KB each, as the interface module, which qualifies the entire FIFO to behave as a standard FIFO.

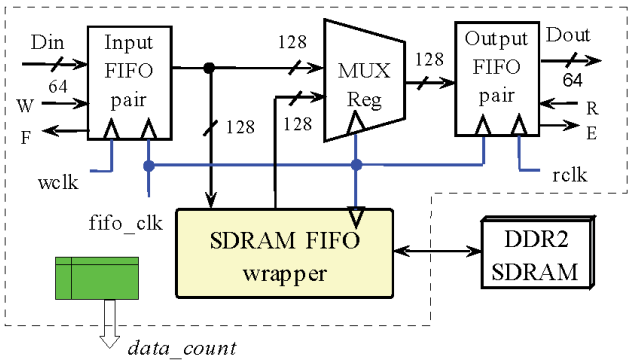

Figure 1: Large-size FIFO block diagram

Development notes

1) Data into and out of the SDRAM module are aligned to the row boundary, to have a better and simplified management over the SDRAM module. Only when the data amount in the small input FIFO block reaches a row size of the DDR2 SDRAM, is the data transfer into the FIFO wrapper executed. And on the other side, only after the output FIFO is able to accommodate a row-size data, is the data directed from the SDRAM to the output FIFO. The advantage lies in minimized row-open and row-close operation for the SDRAM module.

2) Internal data run in double-width data bus, i.e. 128 bit bus, which suffices the possibly full data rate, even if the SDRAM overhead, such as auto refresh and row recharge, have to be taken into account.

3) The PAD delays are variable and calibratable, so that the design has a general application scope to variety of boards. On the Xilinx Virtex5 LX110T FPGA board, IODELAY is used with variable delay value adjustment.

4) The clock frequency for the SDRAM module is some percent higher than the external FIFO clock frequency, to compensate the SDRAM operation overhead such as refresh, recharge. In the ABB2 system, we use 166 MHz as the the kernel clock rate and accordingly, the PCIe DMA fabric logic clock rate is 125 MHz.

5) The data count must be additionally built. Data count is for DMA read logic to determine when to issue the request and for software to know how many data are ready in the Active Buffer.

Test and verification

Timing performance can go easily to over 125 MHz for Virtex5 FPGA with speed grade -1. The numbers of flip-flops and (4-input) look-up-tables used for this FIFO wrapper are both under 1000 and the number of 18Kb RAM blocks is 4. For the adjusting of data bus arrival of the SDRAM module, 4 IDELAYCTRLs are used. Simulation and real test work very well. Additionally we make a standalone test design intensely targeting the FIFO behavior. In a long and sustained test with manual button presses, the FIFO behaves very well in terms of performance and stability. The peak bandwidth goes to 125MHz $\times$ 2 $\times$ 32bit = 8 Gbps in the system. Figure 2 is an example snapshot from ChipScope analyzer.

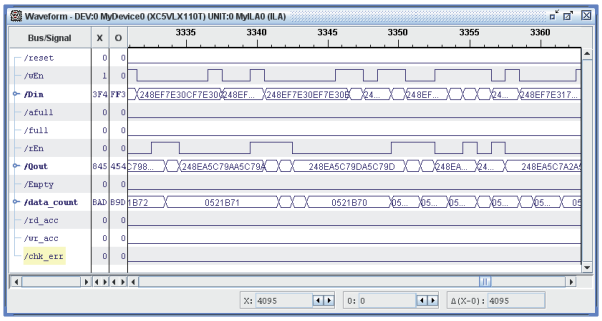

Figure 2: DDR2 SDRAM FIFO behavior

The newer version logic of PCIe DMA integrated with this large-size FIFO works well in system and is verified in the COSY beam test at FZ Jülich in December 2010.

References

[1] W. Gao *et al.*, *CBM Progress Report 2008*, Darmstadt 2009, p. 58